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LINE ITEM NO. 8

DEVELOPMENT OF HIGH EFFICIENCY (14%) SOLAR CELL ARRAY MODULE

FINAL REPORT

FOR PERIOD COVERING

NOVEMBER 1979 TO JUNE 1980

By

P.A. ILES, S. KHEMTHONG, S. OLAH, W.J. SAMPSON, AND K.S. LING

JPL CONTRACT NO. 955217

OPTICAL COATING LABORATORY, INC.
PHOTOELECTRONICS DIVISION
15251 EAST DON JULIAN ROAD
CITY OF INDUSTRY, CA. 91746

"The JPL Low-Cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effect toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by Agreement between NASA and DOE".

ABSTRACT

Most effort was concentrated on development of procedures to provide large area (3" diameter) high efficiency (16.5% AM1, 28°C) P+NN+ solar cells. Intensive tests with 3" slices gave consistently lower efficiency (13.5%). The problems were identified as incomplete formation of an optimum back surface field (BSF), and interaction of the BSF process and the shallow P+ junction. The problem was shown not to be caused by reduced quality of silicon near the edges of the larger slices.

Towards the end of the contract, a promising process sequence was identified, to meet the original goals and tests of this sequence are continuing outside of this program. Despite these problems, a reasonably large number of fairly efficient (13.5% average) 3" P+NN+ cells were made and combined with no problems with the module design developed for this project. In the module, one hundred and twenty (120) cells were connected, eight (8) in parallel and fifteen (15) in series. Six (6) modules were delivered with an average power output (per total module area of 6890 cm^2) of 75.3 watts and a module overall average efficiency of 10.9%.

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1.0 INTRODUCTION

The goal of the program was to design, fabricate and deliver six (6) high efficiency modules, approximately 2'x4', with a nominal output of 96.5 watts at AM1 and 28°C, and (design goal of 14% overall efficiency). The modules were to use P+NN+ cells, and most of the effort was applied to develop procedures to make large area (45.5 cm^2) P+NN+ cells of adequate efficiency (16.5% AM1, 28°C). (The module and cell goals are shown in Table 1.) Complementary effort designed the module layout, and developed tooling for module fabrication, principally for interconnections, white reflecting back surface, back contact soldering machine, AR contact tooling, and assorted tooling for handling and testing, especially for a limited production run.

2.0 TECHNICAL DISCUSSION

2.1 Background

Early work included the possibility that either N+PP+ or P+NN+ cells could be used to achieve the array power goals. However, to provide a possible use for N-type silicon should this type be available at low cost in the future, JPL decided that the main emphasis on this contract should be on P+NN+ cells. There have been some reports in the literature which has shown high performance from the P+NN+ structure (references 1-3). Generally these results were achieved on cells $\leq 4.5 cm^2$ area. In 1970, lithium-doped P+NN+ cells (made by Heliotek or Centralab (1)) achieved 15% AM1, without advantage of some of the later process optimization, including large active area with very fine grids, surface texturing or

TABLE I

MODULE AND CELL PERFORMANCE (ROUND CELLS)

Goal - 14% Module Efficiency:

Module Output =	**96.5W (1)**
Cell Output =	**0.751W (2)**
Cell Efficiency =	**16.5% (2)**

Minimum Module Requirements and Characteristics:

Total Module Area =	6890 cm^2
Cell Packing Factor =	79%
Module Output =	90.0W (1)
Cell Output =	0.701W (2)
Cell Efficiency =	15.4% (2)
Module Efficiency =	13.1%

NOTES: (1) Performance at 100mw/cm^2, AM1 and 28°C.

(2) Assumes 7% module reflectance gain due to white background.

10/80
lr

advanced AR coatings. In 1977, RCA (2) reported cells with 17% AM1, and in 1978 Sandia (3) P/N cells exceeded 17%. In recent years, apart from some interest in improved concentrator cells using the P+NN+ structure, most effort has been given to N+PP+ cells. This was understandable, because this configuration is more radiation resistant for space uses, and also is suited to the probable type (P-type) of future low cost silicon sheets. For the latter, the reduced costs will be achieved partly by fewer purification steps, and boron and aluminum (both acceptors) are the most likely dominant impurities which will remain. The experience with high efficiency, large area (45.6 cm^2) N+PP+ cells led to the choice of a P+NN+ structure, with the N+ processing selected to provide a back surface field (BSF) in addition to a surface N+ layer of increased doping to reduce contact resistance. Again by analogy with earlier work, the target resistivity of the N-silicon was chosen as ~10 ohm-cm, this higher resistivity giving the chance of high Voc (from the BSF) along with enhanced Isc from the higher starting minority carrier diffusion length, and also enhancement of the diffusion length by the BSF.

2.2 Comparison of N+PP+ and P+NN+ Configurations

Theoretically, there is no reason why either of the two configurations N+PP+ or P+NN+ should have higher efficiency. They both use silicon of equivalent quality, and consideration of the main photovoltaic properties confirms this evidence.

Isc - Depends mainly on diffusion length, and in theory and practice, both N and P silicon can have high values. The other factors (reflectance, diffused layer quality) are similar. This equivalent of Isc is seen in the

similarity between the spectral response areas (Figure 1) for good quality cells of each type.

Voc - With or without BSF, Voc values for equivalent bulk-doping levels are close (in theory, Voc for the P/N structure is slightly greater than that for N/P cells because of lower saturation current).

CFF - This is determined mainly by the series and shunt resistances, and these can be optimized in similar fashion for both structures. Thus Pmax which is given by the product Isc . Voc . CFF is equivalent, as is the efficiency. Figure 2 shows I-V curves (at AM0) for good cells of the two types.

2.3 Choice of Process Sequence

By analogy with earlier work and also with current high efficiency N+PP+ cells the BSF option was chosen. The similarities in process sequences can be seen in Tables 2 and 3 which show the flow charts for N+PP+ cells and P+NN+ cell.

2.4 Cell Design

The module design called for the use of 3" diameter (45.6 cm^2 area) cells. This cell size follows current solar cell array practice, and allows the use of standard wafer handling and processing equipment, and current cell technology. However, this choice imposed some limitation on the processses used, and increased the difficulty of achieving high efficiency. The grid contact design for the cell (with a center contact for interconnection) is suitable for sheet resistances 100 ohm/square, and is shown in Drawing A-202337.

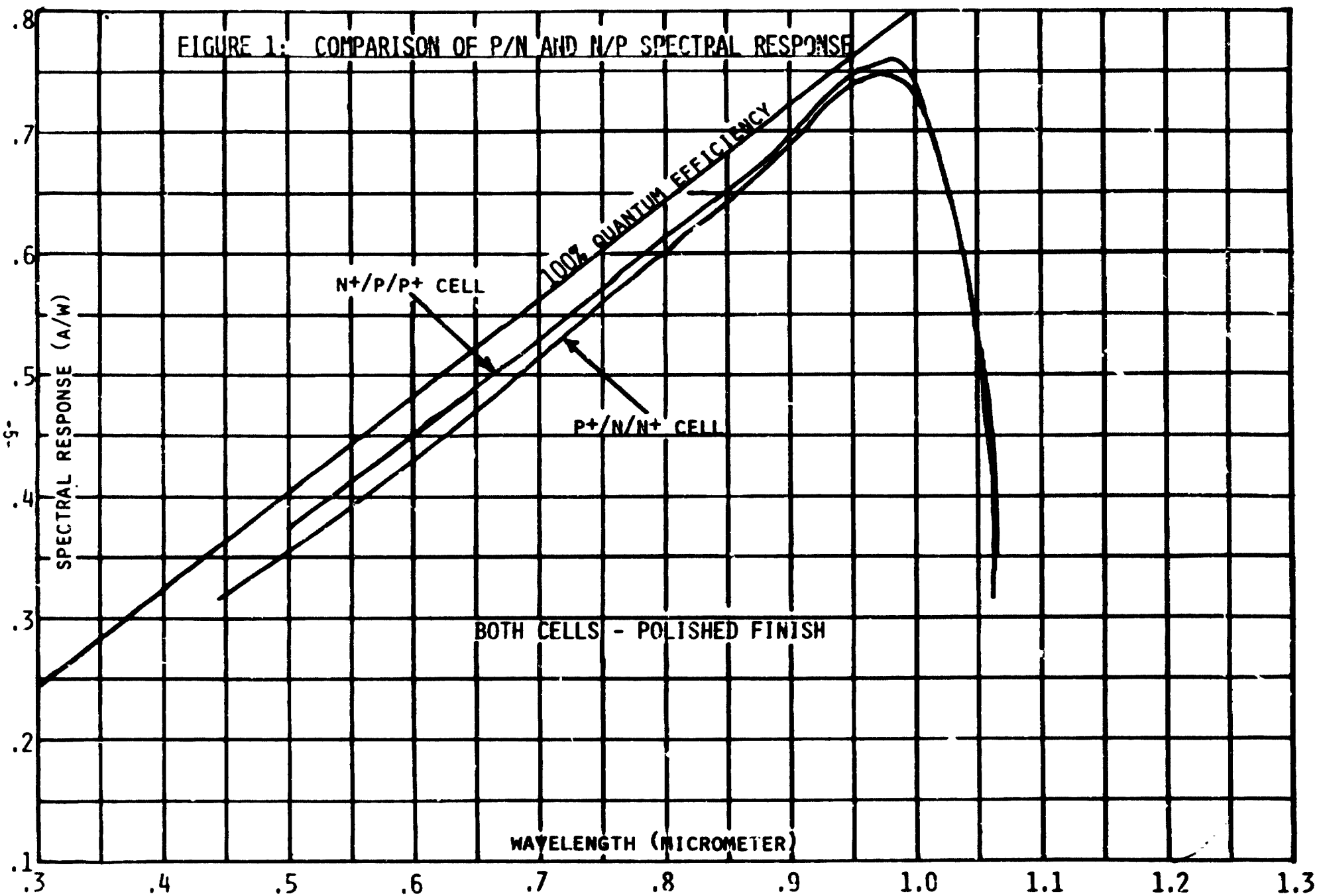


FIGURE 1: COMPARISON OF P/N AND N/P SPECTRAL RESPONSE
100% QUANTUM EFFICIENCY
N+/P/P+ CELL
P+/N/N+ CELL
BOTH CELLS - POLISHED FINISH
SPECTRAL RESPONSE (A/W)
WAVELENGTH (MICROMETER)
.8
.7
.6
.5
.4
.3
.2
.1
.3
.4
.5
.6
.7
.8
.9
1.0
1.1
1.2
1.3

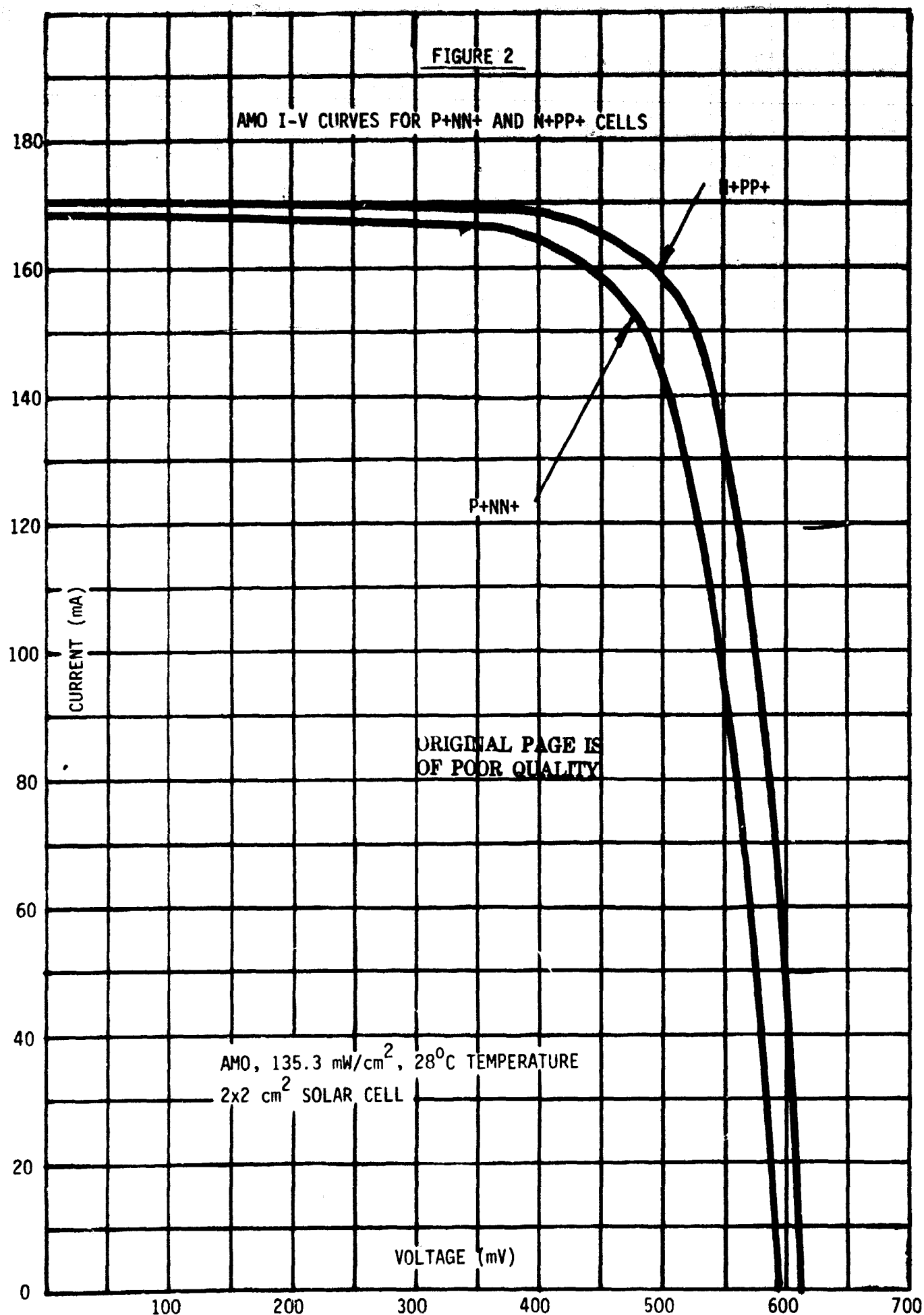


FIGURE 2
AMO I-V CURVES FOR P+NN+ AND N+PP+ CELLS
N+PP+
P+NN+
CURRENT (mA)
VOLTAGE (mV)
AMO, 135.3 mW/cm2, 28°C TEMPERATURE
2x2 cm2 SOLAR CELL
ORIGINAL PAGE IS
OF POOR QUALITY
0
20
40
60
80
100
120
140
160
180
100
200
300
400
500
600
700

TABLE 2

FLOW CHART FOR HIGH EFFICIENCY CELLS

N+PP+

SILICON PREPARATION	1. GROW INGOT, P-TYPE 7-14 OHM-CM 2. SLICE, POLISH AND CLEAN 2A. (OPTIONAL) TEXTURE
N+ LAYER	3. APPLY DIFFUSION MASK TO BACK 4. DIFFUSE N+ (FRONT), ANNEAL 5. HF CLEAN
P+ LAYER	BSF 6. SCREEN PRINT ALUMINUM ON BACK 7. BAKE 8. ALLOY ALUMINUM (P+) 9. REMOVE EXCESS ALUMINUM AND CLEAN
CONTACTS	10. EVAPORATE BACK CONTACT(ALUMINUM, TITANIUM, PALLADIUM,SILVER) 11. FRONT CONTACT MASK (PHOTORESIST) 12. EVAPORATE FRONT CONTACT (TITANIUM-PALLADIUM-SILVER) 13. METAL LIFT OFF 13A CONTACT BUILD-UP (OPTIONAL)
COATING	14. CUT TO SIZE, CLEAN (IF REQUIRED) 15. EVAPORATE AR COATING 16. SINTER (CONTACTS, COATING)
TESTING	17. MECHANICAL INSPECTION 18. ELECTRICAL TEST

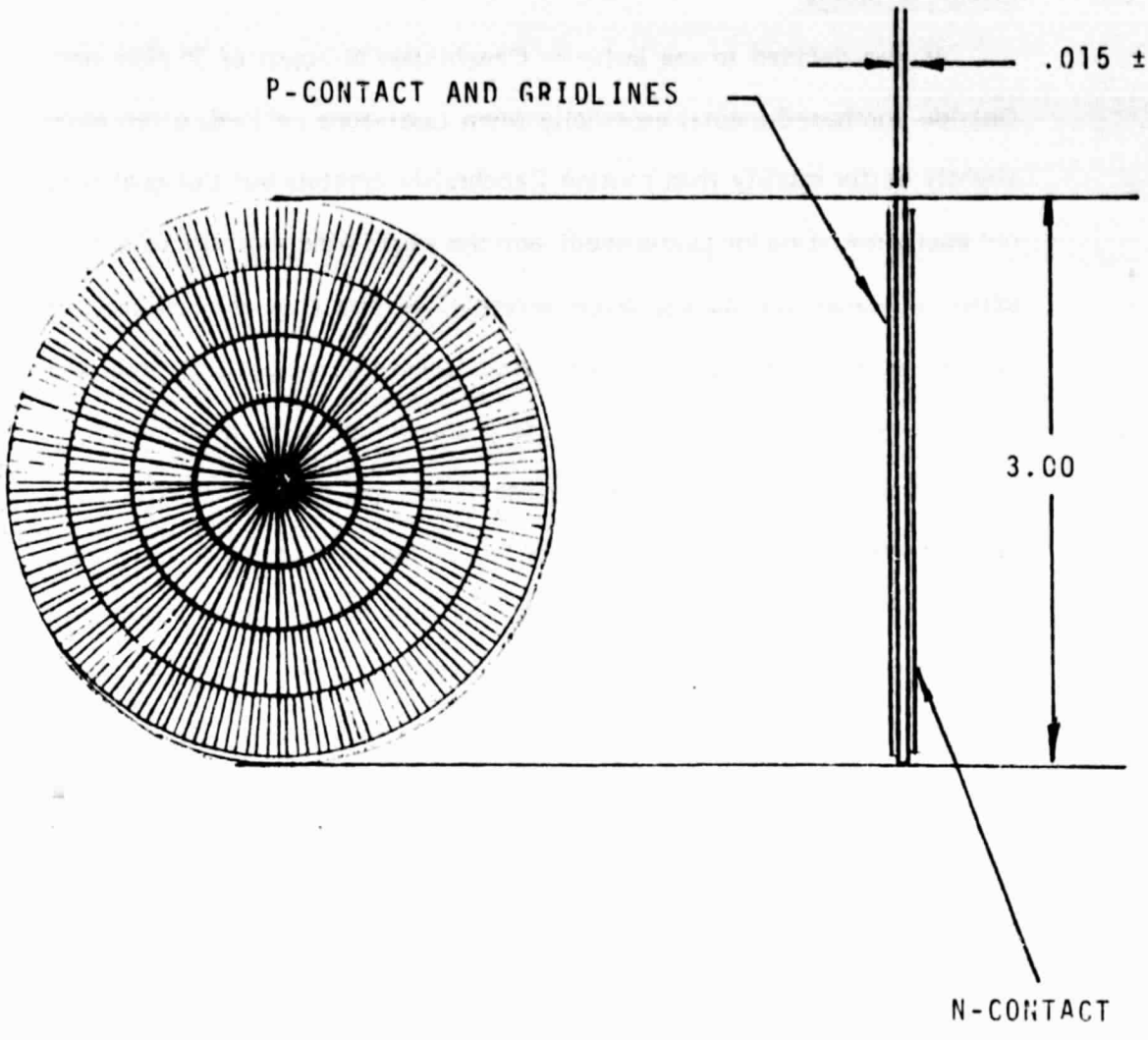
TABLE 3

FLOW CHART FOR HIGH EFFICIENCY CELLS

$P^+/N/N^+$

SILICON PREPARATION	1.	GROW, INGOT, N-TYPE, 7-14 -cm
	2.	SLICE, POLISH AND CLEAN
N^+ DIFFUSION	3.	DIFFUSE N^+ ON BOTH SIDES, ANNEAL
	4.	HF CLEAN
TEXTURING	5.	DEPOSIT CVD OF SiO_2 ON ONESIDE AND EDGE TO PROVIDE DIFFUSION MASK.
	6.	TEXTURE (FRONT SIDE)
	7.	POST TEXTURING CLEAN
P^+ LAYER	8.	DIFFUSE P^+, TACK ON - DRIVE-IN-ANNEAL
	9.	HF CLEAN (REMOVE SiO_2)
CONTACTS	10.	EVAPORATE BACK CONTACTS (TITANIUM, PALLADIUM, SILVER)
	11.	FRONT CONTACT MASK (PHOTORESIST)
	12.	EVAPORATE (TITANIUM, PALLADIUM, SILVER)
	13.	METAL LIFT-OFF
	13a.	CONTACT BUILD-UP SILVER (OPTIONAL)
COATING	14.	CUT TO SIZE (OPTIONAL), CLEAN
	15.	EVAPORATE AR COATING
	16.	SINTER
TESTING	17.	MECHANICAL INSPECTION
	18.	ELECTRICAL TEST

APPLICATION		REVISIONS				
NEXT ASSY	USED ON	LTR	DCN	DESCRIPTION	DATE	APPROVED
		N/C	4374	NEW	1/27/78	



1.0 P-CONTACT OF .25 DIAMETER IS AT CENTER OF CELL

2.0 BOTH CONTACT-METALS ARE VACUUM DEPOSITED TITANIUM-PALLADIUM-SILVER

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS X ±
XX ± .010
XXX ±
FRACTIONS ±
ANGLES ±
DO NOT SCALE DRAWING

DRAWN	S. Khemthong	11/27/78
CHECK		
ENGR	S. Khemthong	11/27/78
PROD		
QA		

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HIGH EFFICIENCY 3" TERRESTRIAL CELL

MATERIAL	SIZE	CODE IDENT NO.	DWG NO.
SILICON SOLAR TERRESTRIAL CELL	A		A-202337

SCALE	REV	SHEET
NONE	N/C	1 OF 1

2.5 Choice of Silicon

It was decided to use in-house Czochralski N-ingots of 3" diameter. Outside purchased-ingots, especially when float-zone refined, often have slightly better quality than routine Czochralski crystals but this quality is not easily specified (or guaranteed) and the world wide shortage of silicon often increases the buying price severely, or stretches the delivery to prevent schedules being met. We could foresee some possible problems when using in-house N-ingots. These problems are first that the lower segregation coefficient of the donor atoms (phosphorus as planned for use but also arsenic and antimony) means that a smaller fraction of the grown ingot is within a given resistivity range (say 7-14 ohm-cm) than for similar ingots doped with boron, whose segregation coefficient is larger (~1.0). In addition, because the N-ingots must be grown in the same growers used for production runs of P-ingots, fewer N-type runs are made, and the "learning curve" which includes intangibles such as furnace clean up by several successive runs is not followed far enough to ensure quality as high as the more frequent P-type ingots.

Even so, ASEC felt that the quality of in-house N-ingots would be sufficient to meet the contract goals. The (100) orientation was used, to allow for possible texturing by preferential etching. The resistivity goal was 7-14 ohm-cm.

2.6 BSF Formation

We selected a phosphorus N+ diffusion to provide a suitable BSF on the N-silicon. The phosphorus N+ diffusion was done on both sides of the

wafer. The goal is to provide a highly doped N+ layer to the back surface and to extend this layer sufficiently deep into the silicon to provide an effective BSF, giving carrier collection increase by preventing back surface recombination, and also an associated Voc increase. The specification of BS Fields even for N+/PP+ cells is still empirical, in that several methods can be successful often with varying effectiveness. The N+ BSF was formed by a phosphorous diffusion at 875°C for 40 minutes.

The N+ step cannot be viewed as a separate entity. For one thing, the N+ diffusion can possibly decrease the original silicon quality (especially the diffusion length) by the combination of the heating and cooling cycles, and the substitutional introduction of high densities of phosphorus, which is slightly mismatched in size with the replaced silicon atoms. On the other hand, with care, the use of some N+ diffusions, especially the $POCl_3$ process selected for use here, can provide some gettering of impurities, with increased diffusion length or even the chance of improved PN junction quality. In addition the front PN junction is provided by a later P+ diffusion, and the heat treatment (heating and cooling) needed for this step can interact with the effectiveness of the N+ layer (the best empirical diffusion cycles for both P+ and N+ are performed at comparable low temperatures (875-900°).

For this reason,several tests of different heating and cooling cycles, and of reversed order of performance were made; other tests included the use of ion implantation to provide either the N+ layer, the P+ layer or both layers on the same slice. We used the ion implantation and annealing procedures felt to be the best available from this method, but found the

overall cell quality slightly lower than the all-diffused methods. For this reason, and to minimize additional delays caused by trying to optimize a process not performed in-house at ASEC, we retained the all-diffused structure.

2.7 Front Surface Finish

To increase overall output, the front surface of the solar cell was textured. After the phosphorus N+ diffusion was formed on both sides of the wafers the wafers were dipped in a 1 to 1 solution of HF acid and water to remove the diffusion oxide. A mask of SiO_2 was then deposited on one side of the wafers to confine the texturing to one side of the wafers and this mask was used to confine the P+ diffusion to the front surface (textured surface). The texturing was done in a 2% solution of NaOH at ~80-85^{o}C resulting in millions of 3-5 μm pyramids. The wafers were then submerged in an Aqua Regia solution (3 parts HCl and 1 part HNO_3) to remove any metallic contamination contained in the NaOH.

2.8 PN Junction Formation

Previous experience showed that the development of a reliable P+ diffusion step was essential to provide high efficiency, large area P+NN+ cells. There are three boron sources which have given good cells, namely boron trichloride (BCl_3), diborane (B_2H_6) and boron nitride (BN).

Based on experience with photosensors and also diffused P+ layers in N+PP+ cells, we selected the BN method for use in this contract. The method used BN discs, with surfaces conditioned, to provide a good B_2O_3 source for vapor transport to the N wafers held close to the BN discs.

The 3" cells were held in a quartz boat with retaining area. As usual for high output solar cell diffusions, the requirements of very shallow junctions (≤ 0.3 μm) and high sheet impurity concentrations raise the possibility of variable junction quality. In addition it is required that the diffused layer be uniform across the whole slice surface. The cycle chosen (900°C for 25 minutes in N_2 atmosphere, followed by a slow cool down (shut off furnace for 1 hour)) gave good PN junctions although a low temperature was selected (to minimize process interactions) and this often gave a slightly higher sheet resistance than required for the grid designs selected (goal was 50-80 ohm/square, often had 100-150 ohm/square). The higher sheet resistance values, in addition to increasing the losses from lateral current flow to the gird lines, also tended to reduce PN junction quality slightly (by shunting). We used a mask layer on the N+ layer to prevent P+ doping of this layer. In summary, the P+ diffusion step gave fairly repeatable results, with PN junction (and cell) performance adequate to achieve the adjusted efficiency requirements of this program.

2.9 Back Contact

After the two diffusion steps, the slices were cleaned to remove the diffusion glasses or mask layers, and then additionally cleaned to prepare the surfaces for contact application. We used the Ti-Pd-Ag contact system currently considered to be the best available, for reduced contact resistance, low grid line resistance, minimum interaction with the N+ and P+ regions and for probable long field life.

2.10 Front Contact

The grid pattern selected for the P+NN+ cells (Drawing A-202337) is designed to give low resistive losses for sheet resistances up to ~100 ohm/square. Although in the module,the eventual mesh interconnect to the center area will involve an additional shadow loss of 1.5% (total shadow losses ~10%), past experience with high efficiency 3" diameter N+PP+ cells has shown that the increased CFF using the pattern selected can offset this additional shadow loss.

The grid pattern is formed by photolithography which allows the use of narrow lines, with some cross lines (see Drawing A-202337). To increase CFF, the silver layer evaporated on the silicon can be built up by electroplating. The silver layer on the front (and the back) can be directly interconnected by use of solder-coated copper mesh.

2.11 AR Coating

When the silicon surface is polished, the use of a multilayer AR coating (in this case TiOx plus Al_2O_3) can provide low reflectance over the cell response range. The coating layers are designed to provide good optical matching with the encapsulating materials, to retain low reflectance in the module. When the surface is textured, already the silicon reflectance is reduced, and the choice of AR coating becomes less critical. However, we have retained the use of the MLAR on the textured surface, thus providing minimum reflectance. The resultant increase in cell current by using textured surface is 3 to 4% above that of a polished surface with the MLAR coating.

2.12 Sintering

As described above, a sinter step is used to increase adhesion of both contacts and coating. In addition this heat treatment can reduce ultraviolet absorption in the coating, and can also reduce contact resistance. Heating at 400°C for 15 minutes was found to be adequate to perform these functions.

2.13 Electrical Test

All cells made were tested at a solar insolation of 100mW/cm^2, at cell temperature of 28°C, using JPL standard cells to calibrate the AM1 simulator. In addition some AM0 measurements were made on smaller area cells (4 cm^2) to provide additional information on the detailed photovoltaic properties.

2.14 Tests Pursued as Part of the Experiments

Use of Ion Implantation to Provide P+ Layer

Spire Corporation implanted B^{11} to form a P+ layer; the BSF was formed either by N+ diffusion (at ASEC) or by P^{31} implantation (at Spire). The best state-of-the-art values for ion energy and fluence were used (10-25 Kev, 2.5-5x10^{15}/cm^2) along with the best combined furnace annealing cycles. The best results (see Table 4) were obtained with the higher energy, higher fluence B^{11} implant, and the N+ diffused layer. However, the results did not show any advantage over all-diffused cells. Because further iterative tests between the two companies would be time-consuming, this option was discontinued for the present program.

TABLE 4

ION IMPLANTATION TESTS,* ($45.6 cm^2$)

TEST	BSF	P+	NO. CELLS	AVERAGE				BEST
				V_{OC}	J_{SC}	CFF	EFF.	EFF.
1. (A)	N+ DIFFUSED	B^{11} IMPLANT 2.5×10^{15} 10 KEV	10	558	33.1	.68	12.5	13.2
2. (B)	N+ DIFFUSED	B^{11} IMPLANT 5×10^{15} 25 KEV	10	570	33.6	.72	13.9	15.0
3. (A)	P^{31} IMPLANT	B^{11} IMPLANT 2.5×10^{15} 10 KEV	10	549	30.4	.65	11.0	11.4

(A) ANNEAL (850-30) + (500-60)

(B) ANNEALED DURING N+ DIFFUSION

* Test Conditions: $28^{\circ}C$ and 100 mW/cm^2

Use of Hydrogen Injection During BN Diffusion

Literature reports suggested that improved consistency could be obtained with BN sources if hydrogen was injected with the other transport gases. Two tests were made, where a small amount of hydrogen (4% by volume) was added to the $N_2 + O_2$ gases during the boron diffusion at 900°C. In test #1, the wafers were given a drive-in cycle in $H_2 + O_2$ atmosphere at 900°C for 25 minutes; in test #2, the drive-in time was 10 minutes. These tests did not show promise, and further tests with hydrogen injection were not pursued, particularly since the tests involved interaction with production diffusion furnaces, the only available equipment for boron diffusion of 3" wafers.

3.0 PRODUCTION RUN

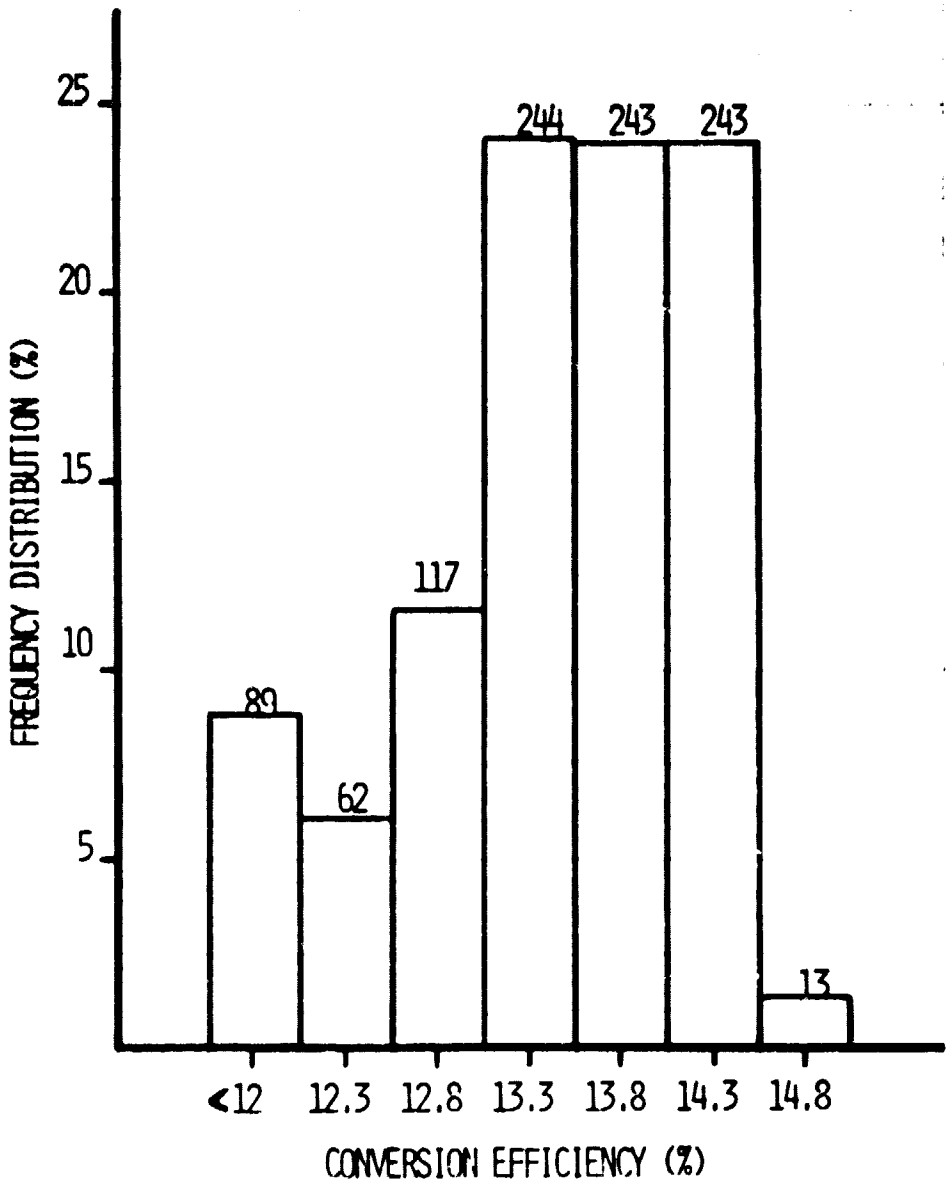
3.1 Amended Goal

In order to meet the original module efficiency goal of 14%, the P+NN+ solar cell efficiency had to be 16.5% at solar insolation of 100 mw/cm^2, 28°C. Due to the difficulties in achieving cell efficiency of 16.5%, it was agreed between JPL and ASEC that the highest efficiency cells achieved to date (~13.5% average) were to be used to produce the modules.

The optimum cell process was chosen and 1,112 cells were processed. One thousand and eleven (1,011) cells were tested at 100 mw/cm^2, 28°C and the electrical distribution is given in Figure 4. Nine hundred and twenty-two (922) cells (91%) had efficiency above 12%, and for these cells, the average efficiency was 13.5%

FIGURE 4: EFFICIENCY DISTRIBUTION OF 1011 - 3" DIAMETER P+NN+ CELLS TESTED AT 100mW/cm^2, 28°C

AVE. EFF = 13.5%

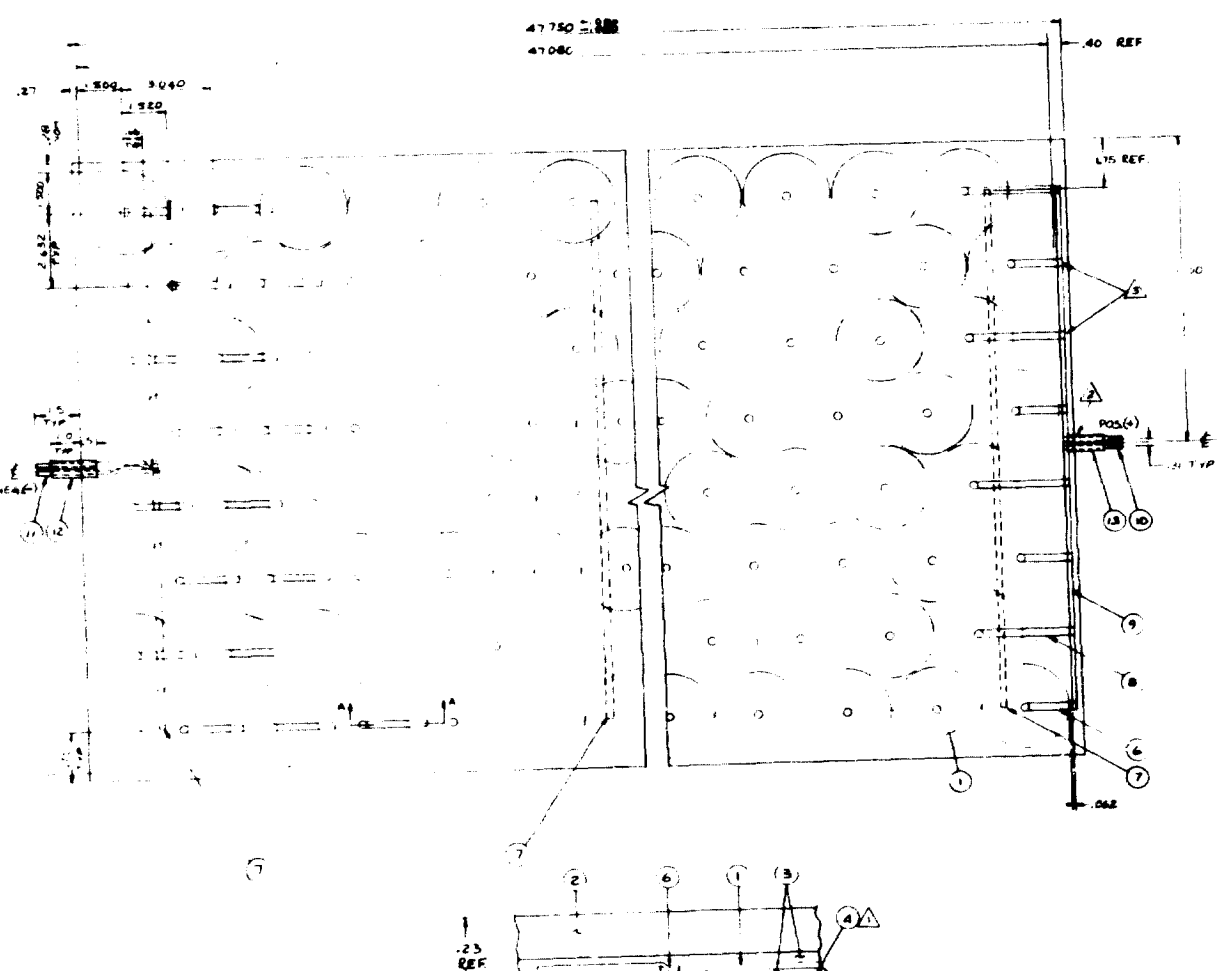


3.2 Cell Assembly

The cell assembly, as shown in Drawing No. D-202373, consisted of (120) 3" cells, connected eight (8) cells in parallel and fifteen (15) cells in series. The parallel connections created three (3) series blocks as shown in Drawing No. B-202374. Each block was made-up of five (5) cells in series by eight (8) cells in parallel for a total of forty (40) cells per block. This particular configuration was a result of JPL recommendation to enhance module reliability and alleviate hot spots in the event of a cell being shadowed or damaged.

3.3 Module Design

The final module design consisted of an aluminum open back frame welded at the corners. The superstrate was 3/16" annealed, edge-ground Sunadex glass. One hundred twenty (120) high efficiency P+NN+, three (3") inch diameter solar cells were encapsulated to the superstrate with polyvinyl butyral (PVB) and covered with white tedlar on the back. The encapsulated assembly was attached to the frame with aluminum hold down angles that were riveted to the welded aluminum frame. A silicone sponge gasket was attached to the frame and another to the hold down angles. This provided a cushion for the encapsulated assembly and a moisture seal. The entire encapsulated assembly was also sealed around the edges with Proglaze, a silicone sealant to insure a good moisture barrier. Electrically, the module was connected with eight (8) strings in parallel by fifteen (15) cells in series. Pigtail output leads secured within a junction box, were used for the electrical termination. The positive lead was at one end of the module and negative at the other. When assembled the module is 48"x22.25"x1.875" and weighs approximately twenty five (25) pounds.



SECTION A-A

NOTES.

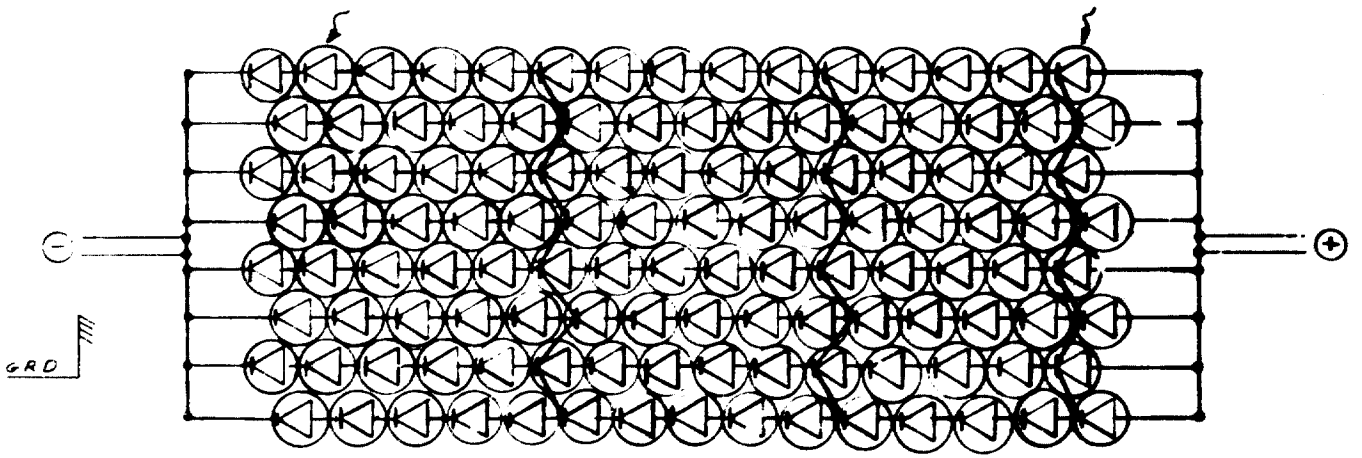
1. APPLY PRIMER TO THIS SIDE OF MYLAR
2. PUSH ITEM 3 AGAINST ITEM 7 DURING SOLDERING OPERATION
3. AFTER MAKING SOLDER CONNECTIONS OF ITEMS 6 & 7 TO ITEM 3, TRIM 6 & 8 FLUSH
4. ITEM NO 7 TO BE SOLDERED AT EVERY CELL ACROSS WITH A 1/4 FOUR ROW SKIP BETWEEN EACH INTERCONNECT.

120	A802337	3" DIA SOLAR CELL	

OCLI — 120 CELL ENCAPSULATION — D802373

B202374

REVISIONS					
DCN	ZONE	LTR	DESCRIPTION	DATE	APPROVED
4802		N/C	NEW RELEASE	2-9-79	
5217		A	OUTPUTS WERE AT ONE END	4/9	
5433		B	REVISED & REDRAWN	7/24/79	



		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DRAWN	T. TARP	3-9-79
		TOLERANCES:	CHECK		
		DECIMALS .X ±	ENGR	S.D	3/9/79
		.XX ±			
		.XXX ±	PROD		
		FRACTIONS ±	QA		
NEXT ASSY	USED ON	ANGLES ±	MATERIAL		
APPLICATION		DO NOT SCALE DRAWING			

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WIRING DIAGRAM
120 CELL PANEL

SIZE	CODE IDENT NO.	DWG NO.
B		B202374

SCALE NONE | REV B | SHEET 1 OF 1

3.4 Module Estimates

Six (6) modules were fabricated. The following module performance, with a 7% anticipated reflectance gain included was calculated based on measured cell performance as follows:

MODULE NO.	CELL EFFICIENCY (%) USED	CALCULATED MODULE POWER (WATTS)	CALCULATED MODULE(%)
HE-001	13.5	78.6	11.4
HE-002	13.6	79.3	11.5
HE-003	13.6	79.3	11.5
HE-004	13.6	79.3	11.6
HE-005	13.5	78.6	11.4
HE-006	13.5	78.6	11.4

3.5 Module Data

All six modules were tested in natural sunlight (the parking lot of Applied Solar Energy Corporation). The test data corrected for 100mw/cm^2, 28^{o}C is tabulated below:

MODULE NO.	MEASURED POWER(WATTS)	CALCULATED CELL EFFICIENCY (%)	CALCULATED MODULE EFFICIENCY (%)
HE-001	74.4	13.6	10.8
HE-002	76.0	13.9	11.0
HE-003	75.7	13.8	11.0
HE-004	75.1	13.7	10.9
HE-005	75.1	13.7	10.9
HE-006	75.5	13.8	11.0

I-V curves for these sunlight measurements are shown in Figures 5 through 10. See Table 5 for complete JPL test data.

3.5.1 Module Testing Requirements

The modules were subjected to the following tests as described in Exhibit 1 of Contract No. 955217, Revision C.

FIGURE 5

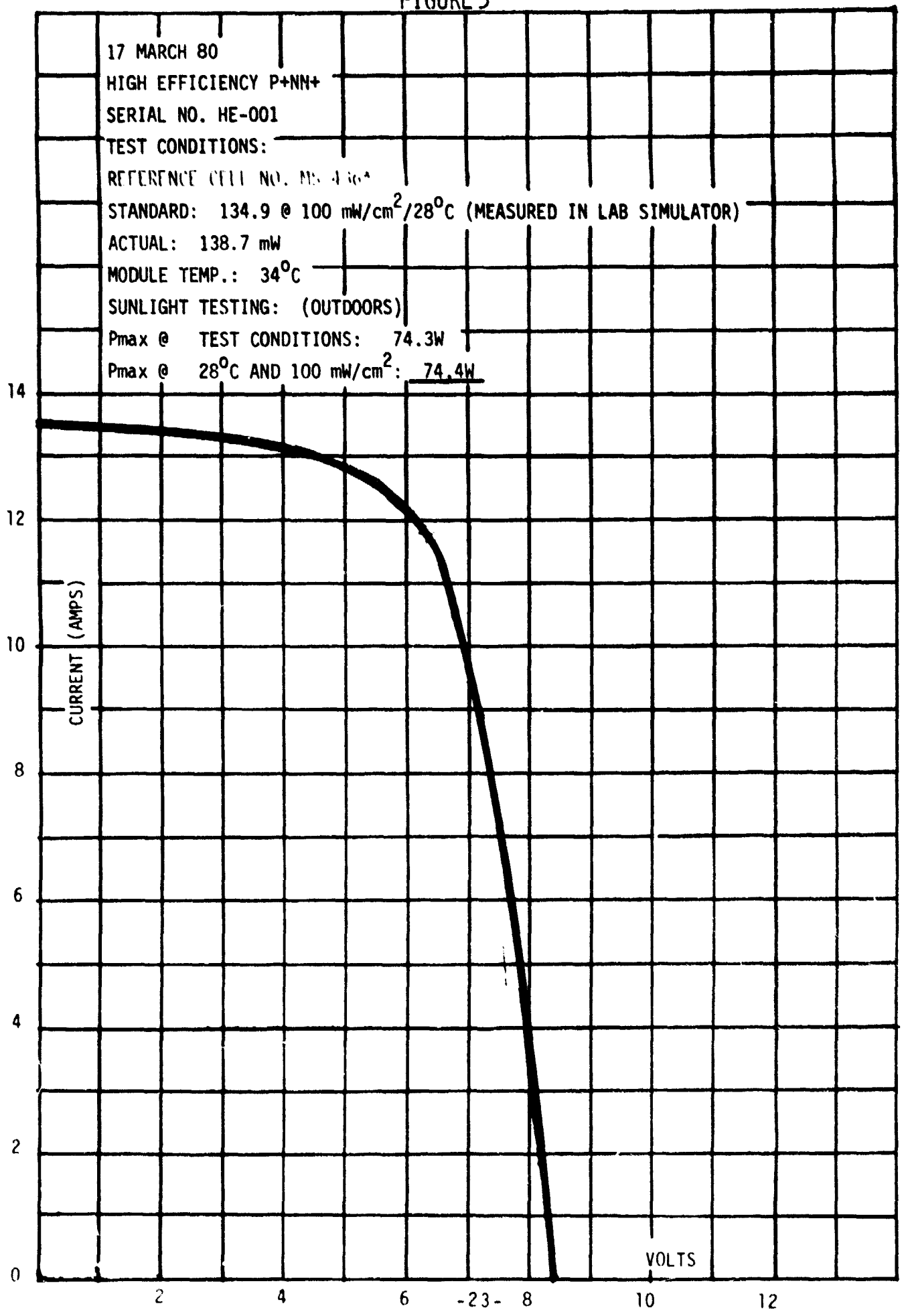

17 MARCH 80
HIGH EFFICIENCY P+NN+
SERIAL NO. HE-001
TEST CONDITIONS:
REFERENCE CELL NO. [illegible]
STANDARD: 134.9 @ 100 mW/cm2/28°C (MEASURED IN LAB SIMULATOR)
ACTUAL: 138.7 mW
MODULE TEMP.: 34°C
SUNLIGHT TESTING: (OUTDOORS)
Pmax @ TEST CONDITIONS: 74.3W
Pmax @ 28°C AND 100 mW/cm2: 74.4W
CURRENT (AMPS)
VOLTS
0
2
4
6
8
10
12
14

FIGURE 6

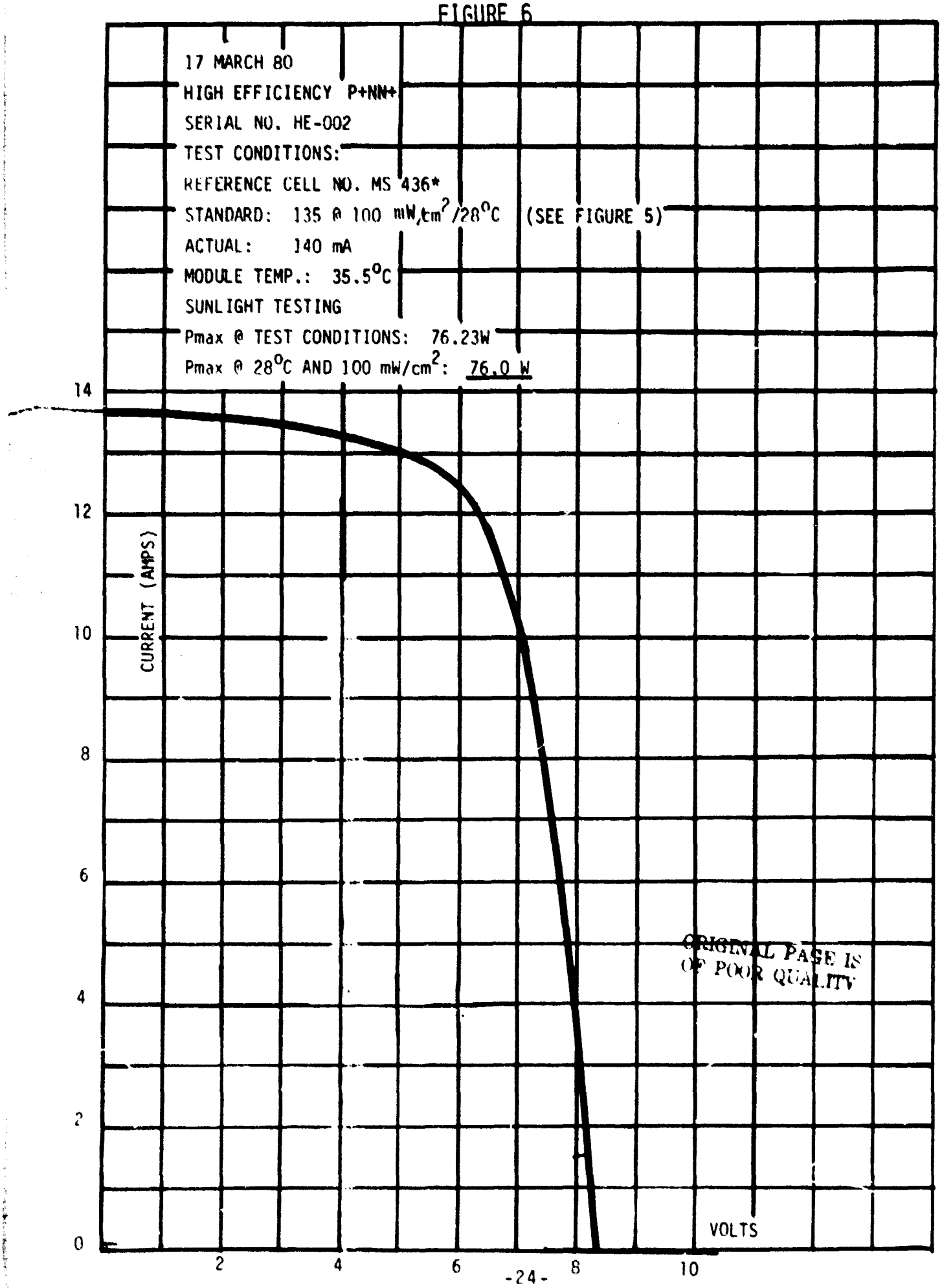


FIGURE 7

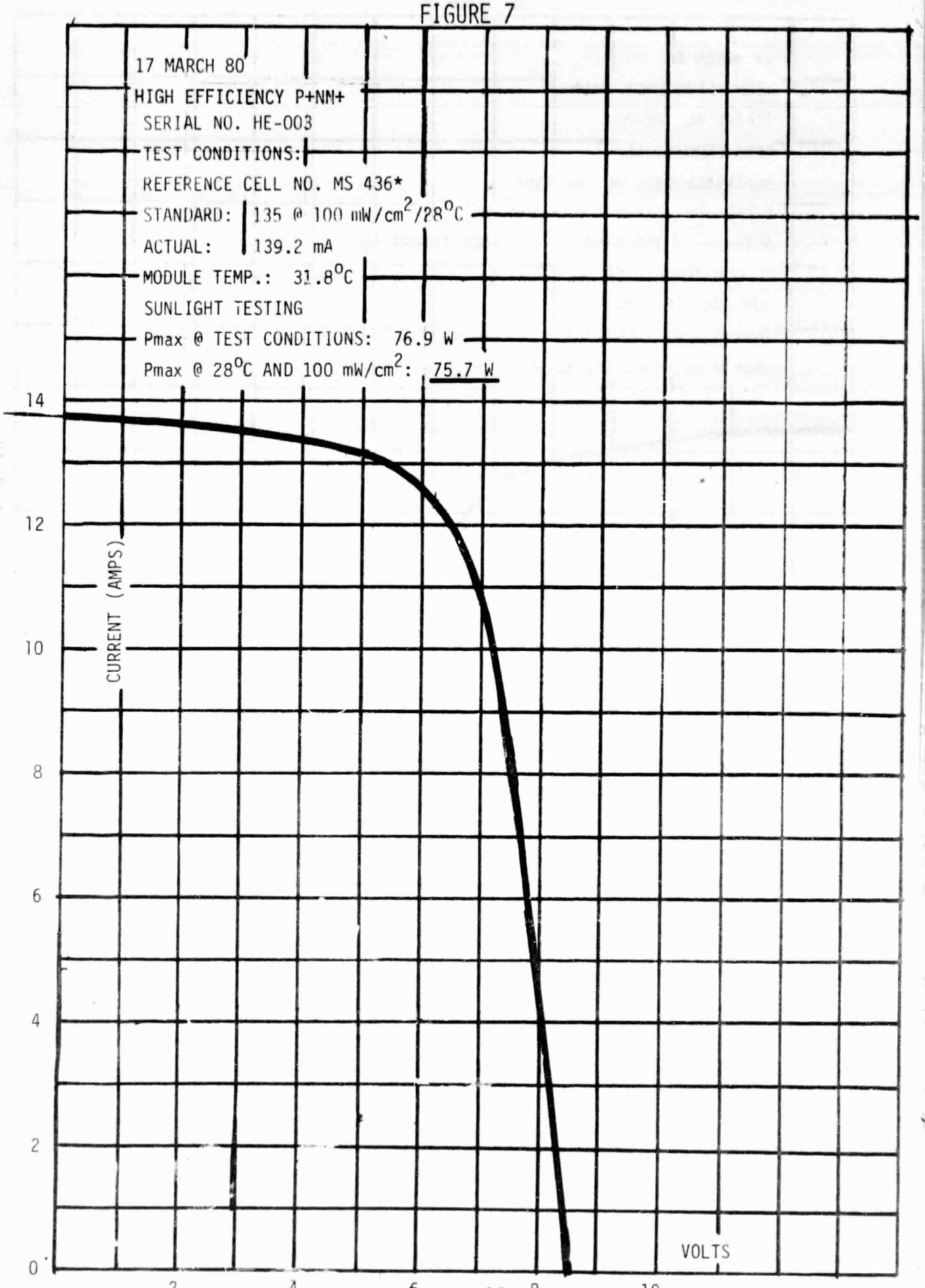

17 MARCH 80
HIGH EFFICIENCY P+NN+
SERIAL NO. HE-003
TEST CONDITIONS:
REFERENCE CELL NO. MS 436*
STANDARD: 135 @ 100 mW/cm2/28°C
ACTUAL: 139.2 mA
MODULE TEMP.: 31.8°C
SUNLIGHT TESTING
Pmax @ TEST CONDITIONS: 76.9 W
Pmax @ 28°C AND 100 mW/cm2: 75.7 W
CURRENT (AMPS)
14
12
10
8
6
4
2
0
2
4
6
8
10
VOLTS

FIGURE 8

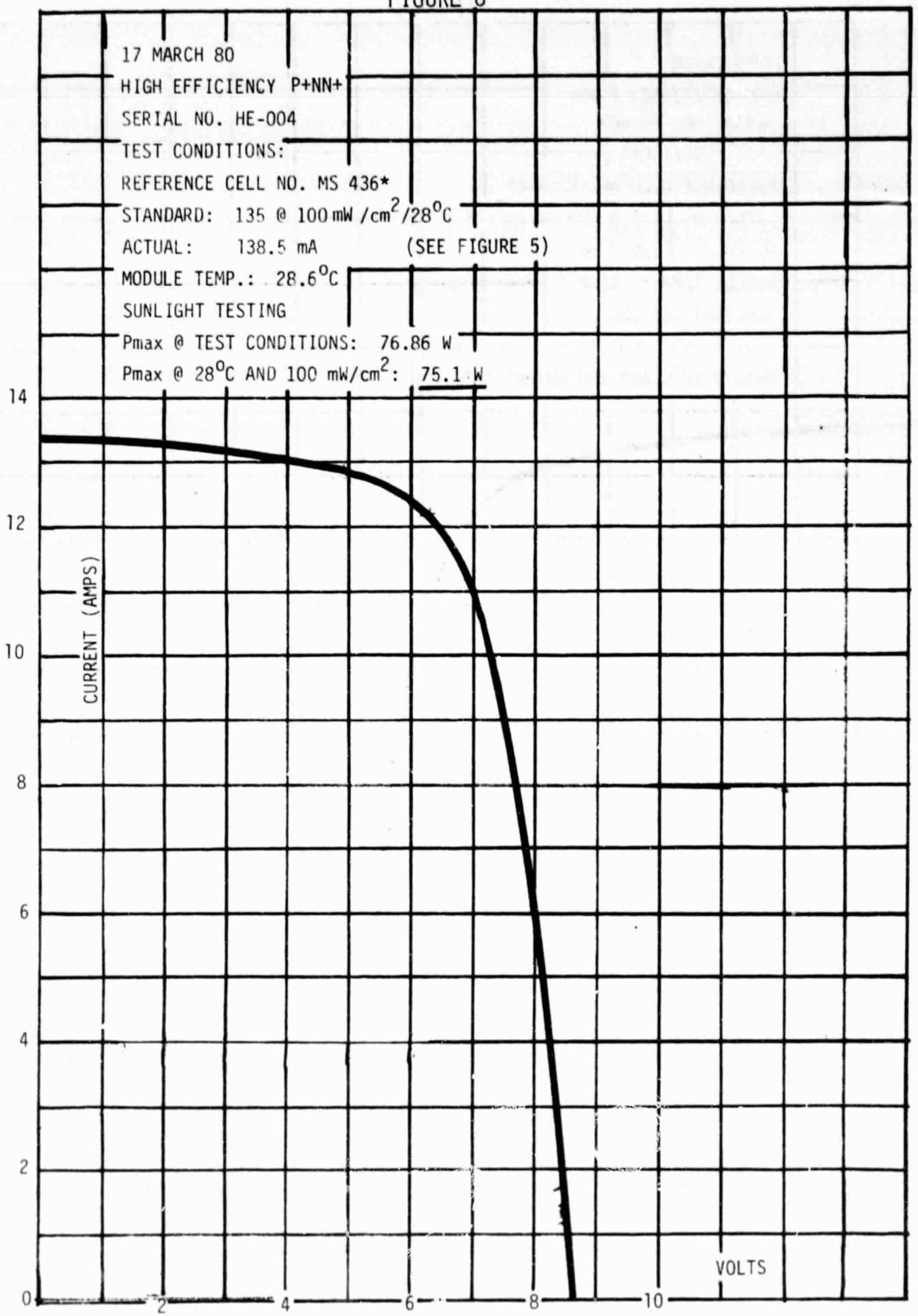

17 MARCH 80
HIGH EFFICIENCY P+NN+
SERIAL NO. HE-004
TEST CONDITIONS:
REFERENCE CELL NO. MS 436*
STANDARD: 135 @ 100 mW /cm2/28°C
ACTUAL: 138.5 mA (SEE FIGURE 5)
MODULE TEMP.: 28.6°C
SUNLIGHT TESTING
Pmax @ TEST CONDITIONS: 76.86 W
Pmax @ 28°C AND 100 mW/cm2: 75.1 W
CURRENT (AMPS)
VOLTS
0
2
4
6
8
10
12
14

FIGURE 9

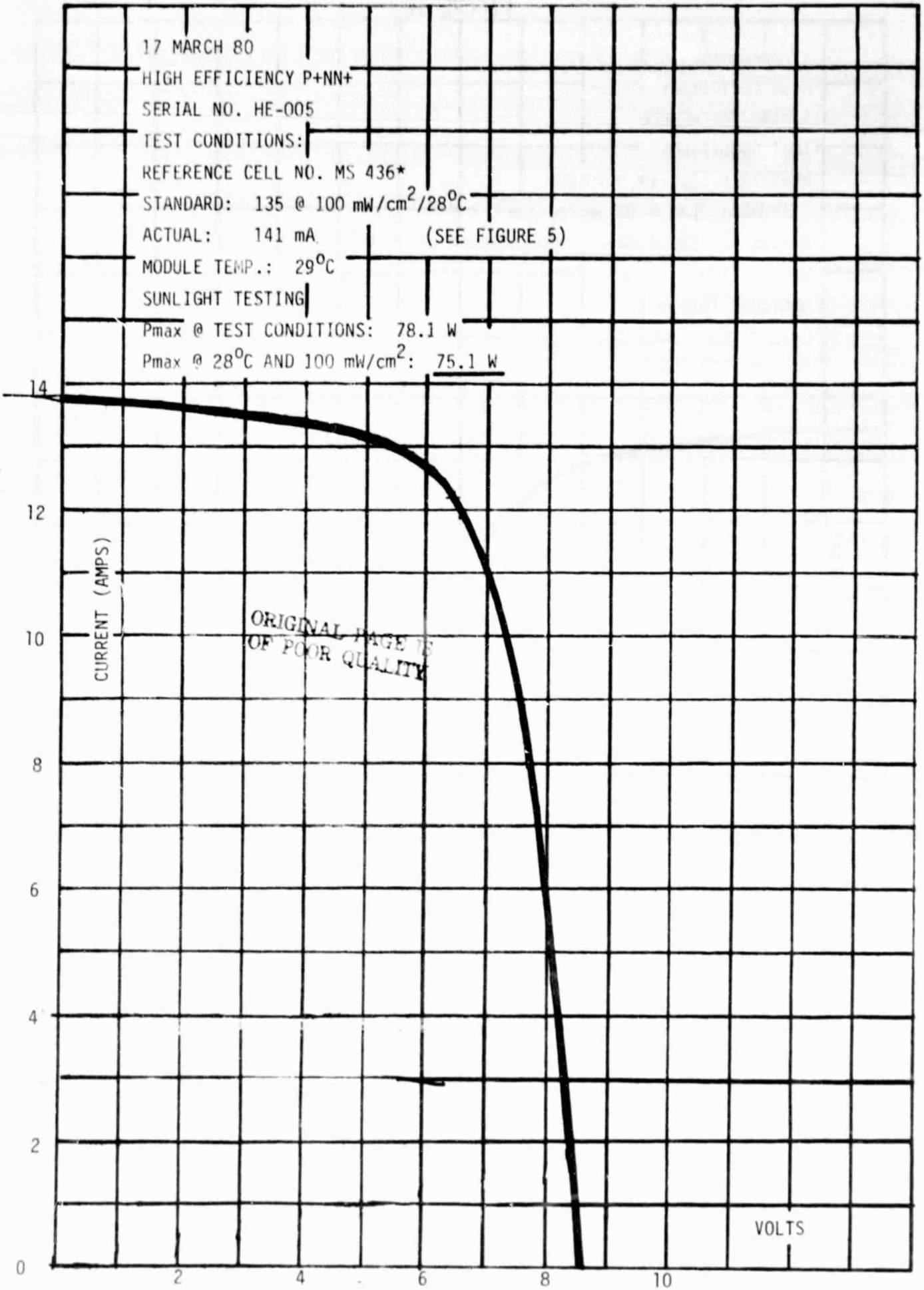


FIGURE 10

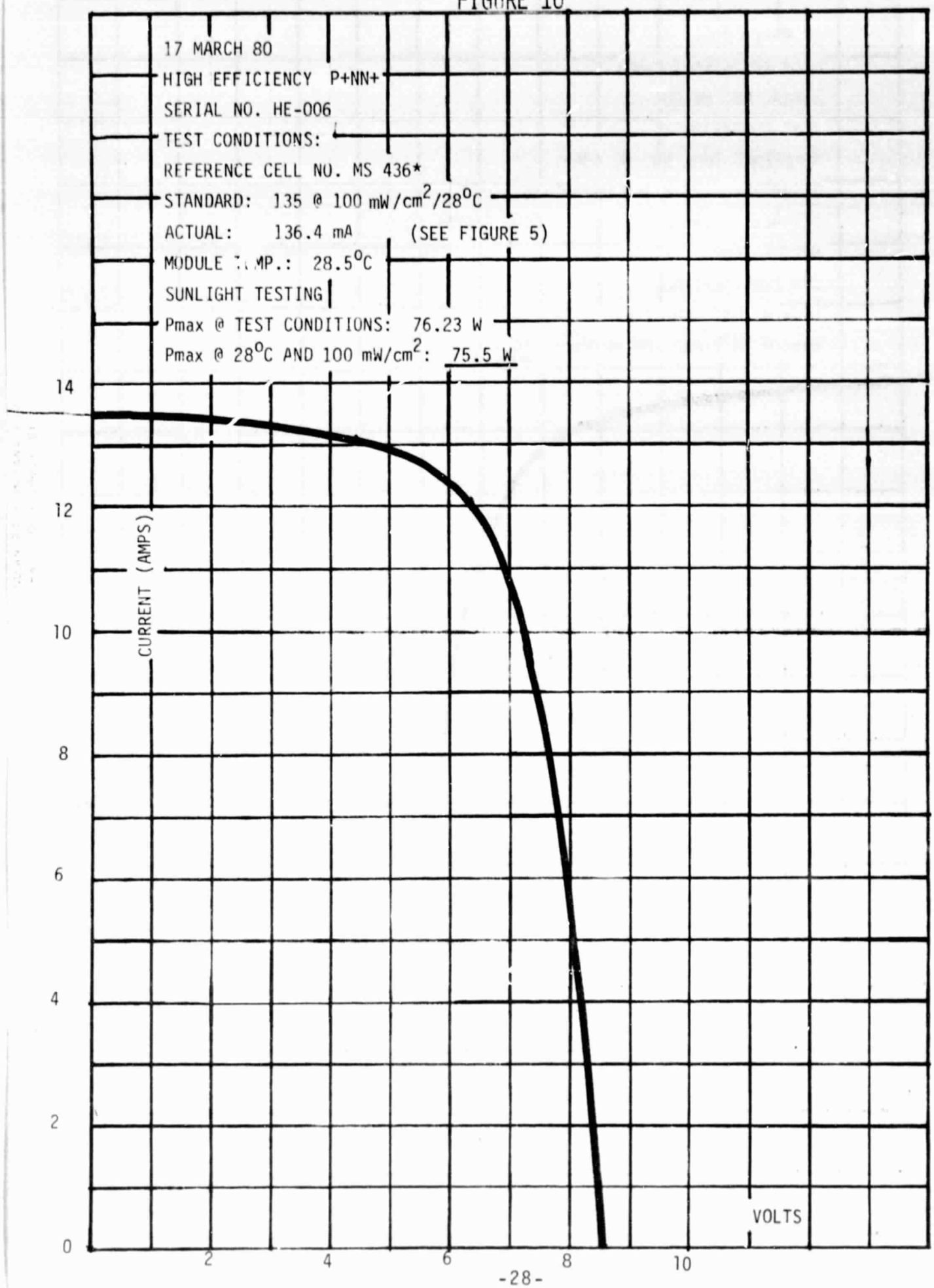

17 MARCH 80
HIGH EFFICIENCY P+NN+
SERIAL NO. HE-006
TEST CONDITIONS:
REFERENCE CELL NO. MS 436*
STANDARD: 135 @ 100 mW/cm2/28°C
ACTUAL: 136.4 mA (SEE FIGURE 5)
MODULE TEMP.: 28.5°C
SUNLIGHT TESTING
Pmax @ TEST CONDITIONS: 76.23 W
Pmax @ 28°C AND 100 mW/cm2: 75.5 W
CURRENT (AMPS)
14
12
10
8
6
4
2
0
2
4
6
8
10
VOLTS

TABLE 5

LSA MODULE TEST SUMMARY

TEST/DURATION
H=HUMIDITY/CYCLES
HL=HAIL/SIZE/INCHES
M=MECH INTEGRITY/CYCLES
S/A=MOUNTED IN SUBARRAY
T=TEMPERATURE/CYCLES

ID NUMBER
LETTERS= MFRER/BLOCK/USE
NUMBER= VENDOR SERIAL NO.

COMMENTS
COEF=TEMP COEFFICIENT
DELAM=DELAMINATION
DSCN=DISCOLORATION
ENCAP=ENCAPSULATION
INTCON=INTERCONNECTOR
DPMC=DELTA PMAX OF CONTROL MODULE
I=IDENTIFIER/J=JPL,V=VENDOR
P/FR=PROBLEM FAILURE REPORT NO.
SAT=COMPLETED TESTS SATISFACTORILY
SBSTR=SUBSTRATE

ELECTRICAL
IMP=CURRENT AT PM,28DEG C,A
ISC=SHORT CKT CURRENT,28DEG C,A
P=POWER AT RATING V,NOCT
PM=POWER MAX,28DEG C CURVE
VOC=OPEN CKT VOLTAGE 28DEG C,V
VMP=VOLTAGE AT PM,V
DELTA,PCT=DIFFERENCE PERCENT
FF=FILL FACTOR,PM/ISC X VOC
FLASH DATE=DATE OF ELEC TEST

VENDOR: ASEC (OCLI)
MODEL D202400-A
PROCUREMENT: PP&E
RATING VOLTAGE: NOT RATED
STATUS AS OF: 07/09/80

ID NUMBER	LINE	TEST DURATION	JPL PM,W	DELTA PM,PCT	FLASH DATE	I	P NOCT	DELTA P,PCT	ISC	VOC	IMP	VMP	FF	P/FR
MRTH-001	1	RECEIVING	71.78		04/24/80									
MRTH-001	2	VENDOR	74.4	+3.7	03/17/80									
MRTH-001	3	S/A-22-2	72.25		05/21/80									
MRTH-001	4	RECHECK	72.12		05/28/80		BASE							
MRTH-001	5	T-50	71.51	-0.8	06/09/80		SATISFACTORY							
MRTH-001	6	H-5	71.13	-1.4	06/19/80		SATISFACTORY							
MRTH-001	7	M-100	70.65	-2.0	06/25/80		SATISFACTORY							
MRTH-001	8	TWIST			06/30/80		SATISFACTORY							
MRTH-001	9	HI-POT			06/30/80		SATISFACTORY							
MRTH-002	1	RECEIVING	72.44		04/24/80									
MRTH-002	2	VENDOR	76.0	+4.9	03/17/80									
MRTH-002	3	PRE-TEST	72.05		05/21/80									
MRTH-002	4	S/A-22-2	72.06		05/28/80		BASE							
MRTH-002	5	T-50	70.85	-1.7	06/09/80		1 CELL CRACKED, 20mm LONG							2234
MRTH-002	6	H-5	71.44	-0.9	06/19/80		SATISFACTORY							
MRTH-002	7	M-100	70.31	-2.4	06/25/80		SATISFACTORY							
MRTH-002	8	TWIST			06/30/80		SATISFACTORY							
MRTH-002	9	HI-POT			06/30/80		SATISFACTORY							
MRTC-003	1	RECEIVING	73.21		04/24/80									
MRTC-003	2	VENDOR	75.7	+3.4	03/17/80		CONTROL MODULE							
MRTC-003	3		75.70		05/21/80		CONTROL MODULE							
MRTC-003	4	RECHECK	73.04		05/21/80		CONTROL MODULE							
MRTC-003	5	RECHECK	73.75		05/28/80		CONTROL MODULE, BASE							
MRTC-003	6		72.91	-1.1	06/09/80		CONTROL MODULE							
MRTC-003	7		73.06	-0.9	06/19/80		CONTROL MODULE							
MRTC-003	8		73.08	-0.9	06/25/80		CONTROL MODULE							

TABLE 5

MRTH-004	1	RECEIVING	74.05		04/24/80		
MRTH-004	2	VENDOR	75.1	+1.4	03/17/80		
MRTH-004	3	PRE-TEST	73.81		05/21/80		
MRTH-004	4	S/A-24-2	73.84		05/28/80		
MRTH-004	5	RECHECK	72.84		05/28/80	BASE	
MRTH-004	6	T-50	71.56	-1.8	06/09/80	SATISFACTORY	
MRTH-004	7	H-5	71.49	-1.9	06/19/80	SATISFACTORY	
MRTH-004	8	M-100	71.41	-2.0	06/25/80	SATISFACTORY	
MRTH-004	9	TWIST			06/30/80	SATISFACTORY	
MRTH-004	10	HI-POT			06/30/80	WITH 750VDC APPLIED, AUTOMATIC SYSTEM DUMPED @ 50 MICROAMPS +.	2230
MRTH-005	1	RECEIVING	73.16		04/24/80		
MRTH-005	2	VENDOR	75.1	+2.7	03/17/80		
MRTH-005	3	PRE-TEST	72.38		05/21/80		
MRTH-005	4	S/A-24-2	69.09		05/28/80		
MRTH-005	5	RECHECK	71.86		05/28/80	BASE	
MRTH-005	6	T-50	71.13	-1.0	06/09/80	SATISFACTORY	
MRTH-005	7	H-5	71.58	-0.4	06/19/80	36mm EDGE CRACK FROM CHIP	2237
MRTH-005	8	M-100	71.02	-2.5	06/25/80	SATISFACTORY	
MRTH-005	9	TWIST			06/30/80	SATISFACTORY	
MRTH-005	10	HI-POT			06/30/80	SATISFACTORY	
MRTH-006	1	RECEIVING	74.57		04/24/80		
MRTH-006	2	VENDOR	75.5	+1.2	03/17/80		
MRTH-006	3	PRE-TEST	73.10	-2.0	05.21/80		
MRTH-006	4	RECHECK	72.30	-3.1	05/22/80		
MRTH-006	5	RECHECK	68.63	-8.0	05/27/80		
MRTH-006	6	RECHECK	69.78	-6.4	05/27/80	UNSTABLE OUTPUT, TO F/A.	2276

A) Qualification Tests

The Tests described herein are intended to characterize the module performance and to provide a high level of confidence that production modules will function within the specified performance requirements in terrestrial environments.

1) Electrical Performance:

The current-voltage (I-V) characteristics of each module were determined and are shown in Figures 5 thru 10.

2) Electrical Insolation Tests:

a) Insulation Resistance Test. The output terminals of the module were shorted together and connected to the high voltage contact of a megometer. The return contact of the test instrument was connected to the module substrate, frame, or grounding terminal. The module was tested in the non-illuminated condition. The insulation resistance was measured after one minute application of +1500 VDC. The test was repeated with the test polarity changed to -1500 VDC. Neither measurement exceed the insulation resistance requirement, a minimum of 100 meg-ohms.

b) Voltage Withstanding Test. All modules subjected to this test. Output terminals of the module were shorted together and connected to the positive supply of an insulation tester. The return circuit of the tester was connected to the substrate, grounding terminal or frame. Voltage was applied at a rate of 500 VDC/sec. in three steps of 500 VDC at 15 second intervals until

reaching 1500 volts and held at that level for one minute. The testing equipment was current limiting at 50 microamps for detection of breakdown initation and voltage interruption. The modules were tested in the non-illuminated condition and there was be no evidence of dielectric breakdown.

3) Environmental Tests:

The environmental tests identified in this paragraph were conducted with each module mounted on a test frame designed to simulate attachment to a rigid support structure.

The electrical performance test and a visual inspection were performed at the beginning and after the completion of each environmental test. The electrical isolation tests were performed both at the start of environmental testing and after the last qualification test. The environmental tests were performed sequentially in the order listed below.

a) Thermal Cycling Test

Each module was subjected to 50 cycles with the cell temperature varying between -40°C and +90°C. The temperature varied approximately linearly with time at a rate not exceeding 100°C per hour and with a period not greater than 6 hours per cycle (from Ambient to -40°C to +90°C to Ambient).

b) Humidity Test

Each module was subjected to the humidity cycling. Electrical performance tests was performed within one

hour after removal from the humidity chamber.

c) Mechanical Integrity Test

Each module was subjected to a cyclic load test in which the module was supported only at the design support points by a rigid fixture, and a uniform load normal to the module surface was cycled from +50 pounds per square foot to -50 pounds per square foot 100 times.

4) Allowable Degradation

The power output degradation determined after completion of the last pre-production acceptance test did not exceed 5% of the power measured in the initial electrical performance test. There was no reduction in the electrical isolation capability as measured by the initial Electrical Isolation Tests. Any observable cracks or other mechanical degradation (such as delamination of coatings or broken elements) were evaluated for acceptability per the Inspection System Plan.

3.6 Superstrate

The annealed, edge-ground Sunadex glass was chosen as the superstrate mainly due to the results published in JPL Report 5101-62 entitled, "Photovoltaic Solar Panel Resistance to Simulated Hail". Annealed glass upon impact would only crack but the module would still

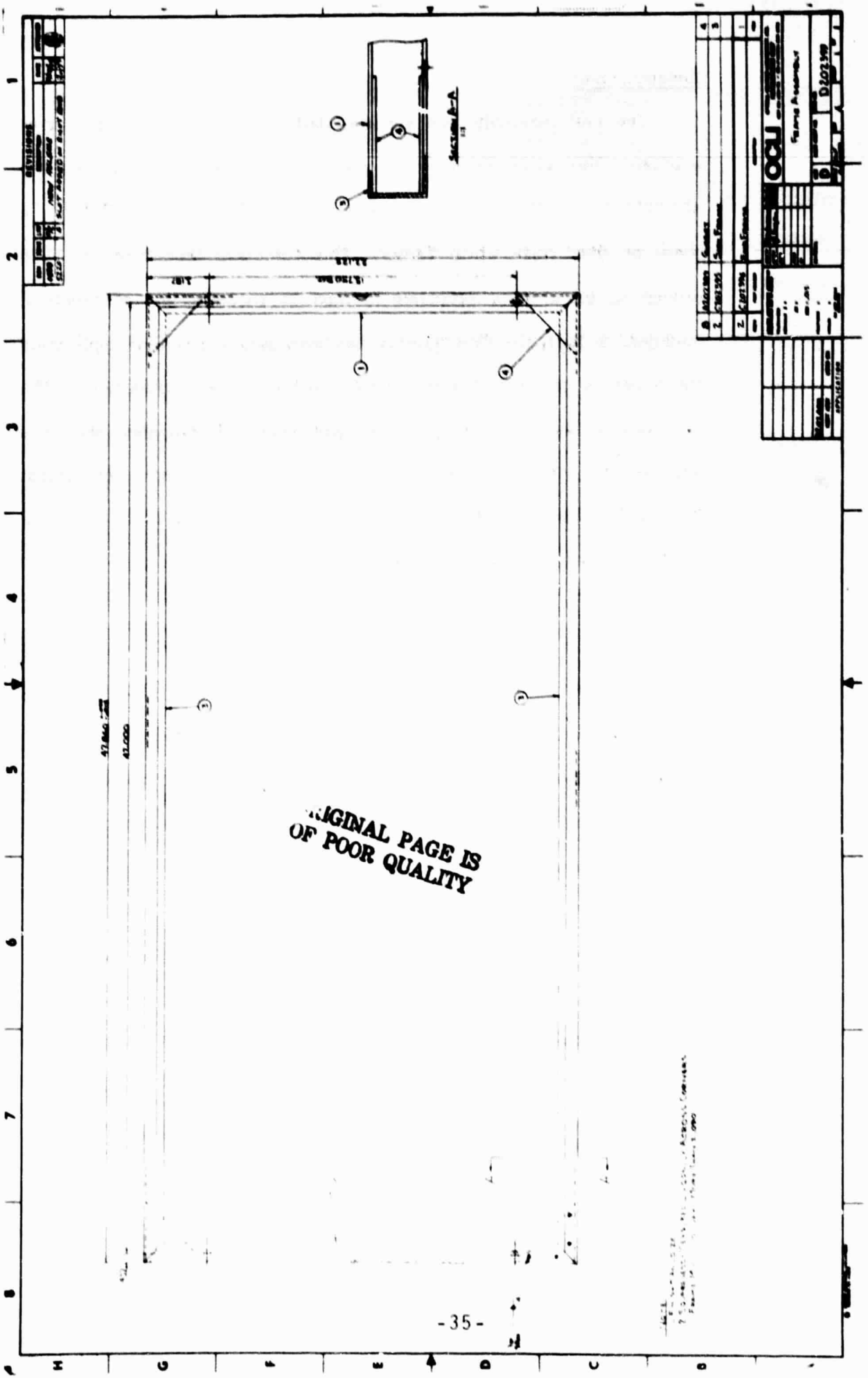
function initially with very small electrical degradation. Tempered glass would shatter upon impact resulting in loss of power output. Even though the mechanical strength of the annealed glass is less than that of tempered glass, it is more than sufficient to satisfy the hail test requirement.

As edge-grinding the edges of the glass improves the performance under the steel ball drop test, ASE decided to use edge-ground glass superstrate.

Sunadex glass was selected because of its high transmission qualities and excellent performance. We have successfully and consistently seen an increase in module power output when using the Sunadex textured surface glass in conjunction with a white background between cells. The extra heavy 3/16" thickness was chosen to insure additional strength. This has been determined to be more than adequate to do the job.

3.7 Module Frame

The module frame is made of 6063-T5 alloy extruded aluminum "C" shaped channel which was miter cut at the corners and welded. Reinforcement gussets are used in each corner to increase strength. The weld beads were ground smooth on both surfaces after welding then the entire frame assembly was coated with a clear anodized finish for surface protection. See Drawing No. #-202399 for a detailed view of this module frame.



3.8 Encapsulation

The cell assembly was encapsulated in a conventional autoclave machine. The system consists of a piece of Sunadex superstrate, a sheet of .015" thick PVB, the cell assembly, a sheet of .015" thick PVB, and a sheet of .004" thick white Tedlar. This autoclave procedure has been proven to be a quite effective method of encapsulating photovoltaic modules. In fact, the PVB material has been used in a similar application for years in the automotive industry without any degradation. The autoclave produces an exceptionally good bond between glass and cells and the PVB withstands thermal cycling quite well. After encapsulation the fragile solar cells and the glass superstrate become an integral, strong assembly that is quite easy to handle.

3.9 Edge Sealing

Until recently, ASEC has produced terrestrial modules using monoacrylic as the edge sealant. During the temperature cycling test between -40°C and +90°C, the Sunadex glass superstrate cracked. It was found that monoacrylic becomes very hard at low temperatures and at the same time, the adhesion to the glass and the aluminum frame is enhanced. The mismatch of temperature coefficients of the glass and aluminum causes the glass to crack. After changing the sealant to Proglaze, the modules passed the temperature cycling test. The Proglaze material is an excellent moisture seal and has very good elasticity at both high and low temperatures. This material has been used in the construction industry for years and has been found to be quite durable in outdoor use.

3.10 Electrical Terminals

For cost effectiveness, the relatively expensive sockets previously used were replaced with two (2) Teflon insulated No. 16 AWG stranded wires secured by two Heyco strain relief clamps as shown in Drawing No. C-202392 as electrical terminals. A separate aluminum junction, box with grounding stud, is supplied for each polarity. The dual positive pigtails are at one end of the module and the dual negative at the other. We have used the dual terminal concept for each polarity to enhance module reliability.

4.0 OTHER ITEMS

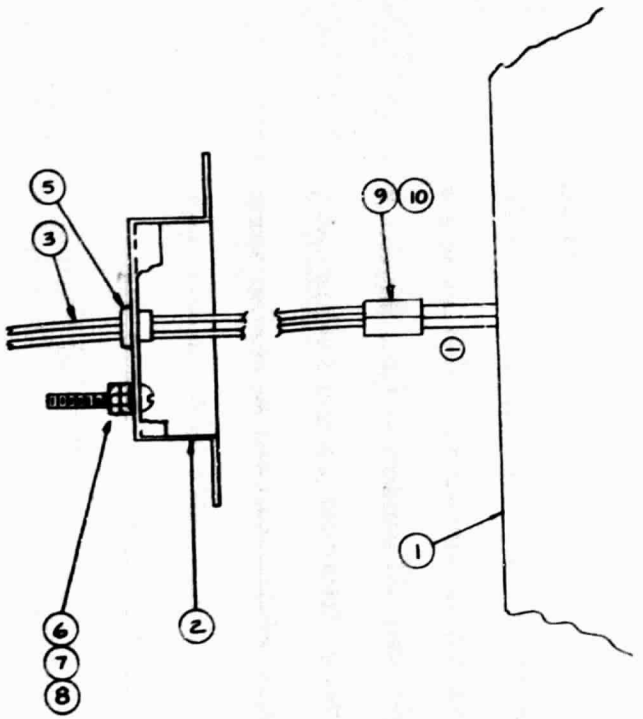
4.1 Reference Cells 2x2 cm^2

Twenty five (25) 2x2 cm^2 P+NN+ reference cells were delivered to JPL in February 1980. These reference cells were part of the production run. The electrical data of these reference cells are shown in Table 6. The average efficiency was 16.2%. These reference cells were tested in ASEC's test facility; the intensity of the test simulator was calibrated by using a reference BSF N+PP+ cell (calibrated by JPL under JPL Contract No. 955409). The spectral response of this N+PP+ reference cell is very similar to those of P+NN+ reference cell. Despite the high efficiency, Voc was still slightly lower than the best values observed.

4.2 AR Coating Anomaly

Towards the end of this work, an anomaly was noted when textured P+NN+ cells were AR coated. The Isc increased as expected (8.7% for MLAR coating and 6% for SiO or spin-on liquid coating prepared by

REVISIONS					
DCN	ZONE	LTR	DESCRIPTION	DATE	APPROVED
4681		NC	NEW RELEASE	5/3/79	
5218		A	REDESIGN FOR 2 J BOXES	7/1/79	



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C202392

REQ'D	PART NUMBER	DESCRIPTION	ITEM
AR		SOLDER JOINT ALLOY 60/40	10
4		TEFLON HEAT SHRINK INSUL. 3/16 x 1" 8 MIL	9
4		#6-32 HEX. NUT (SST)	8
2		#6-32 x 1/4 R.H. MACH. SCR (SST)	7
4		#6 STAR LOCK WASHER	6
2		STRAIN RELIEF - HEYCO # SP-1	5
2		#24 AWG TEFLON INSUL. HOOK-UP WIRE / 48" (WHITE)	4
2		#24 AWG TEFLON INSUL. HOOK-UP WIRE / 48" (BLACK)	3
2	C202391	JUNCTION BOX	2
1	D202373	20 CELL ENCAPSULATION	1

NOTE:

1. NEGATIVE SIDE WIRING SHOWN. POSITIVE SIDE IS THE SAME EXCEPT ITEM 4, WHITE WIRE IS USED
2. PROVIDE ADEQUATE WIRE SERVICE LOOP IN J BOX.

D202400	
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE ... INCHES
TOLERANCES
DECIMALS X ±
.XX ±
.XXX ±
FRACTIONS ±
ANGLES ±
DO NOT SCALE DRAWING

DRAWN P.S. Whittier 5/30/79
CHECK M.F. Simpson 5/31/79
ENGR
PROD
QA
MATERIAL

OCLI OPTICAL COATING LABORATORY, INC. PHOTOELECTRONICS GROUP
1900 Charleston Rd. • Santa Clara, California 94042

JUNCTION BOX
TERMINAL WIRING

SIZE C | CODE IDENT NO | DWG NO C202392
SCALE NONE | REV A | SHEET 1 OF 1

TABLE 6

SOLAR CELL ELECTRICAL DATA FOR P+NN+ REFERENCE CELL

(2x2 cm^2, 100 mW/cm^2, at 28°C)

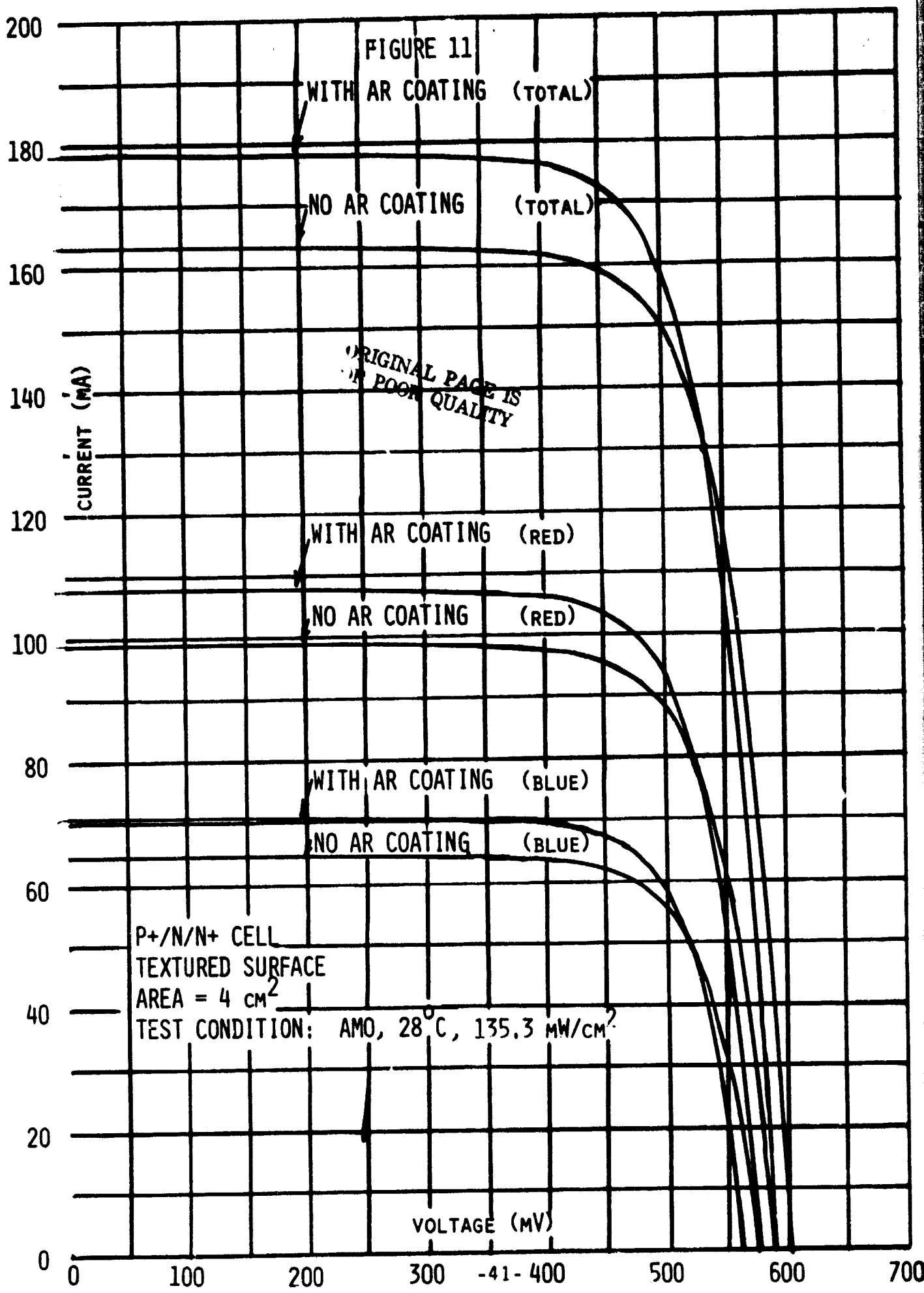
Cell No.	Voc (mV)	Isc (mA)	$I_{1.470}$ (mA)	CFF (%)	(%)
01	574	148.5	137.5	75.8	16.2
02	575	148.5	137.0	75.4	16.1
03	574	149.5	138.0	75.6	16.2
04	575	148.0	136.5	75.4	16.0
05	576	148.0	138.0	76.1	16.2
06	574	149.0	138.5	76.1	16.3
07	576	148.5	139.0	76.4	16.3
08	578	148.5	138.5	75.8	16.3
09	575	149.5	139.0	76.0	16.3
10	575	148.5	137.5	75.7	16.2
11	575	148.5	138.5	76.2	16.3
12	574	146.5	135.0	75.4	15.9
13	576	148.0	138.0	76.0	16.2
14	575	150.0	139.0	75.7	16.3
15	573	148.5	136.0	75.1	16.0
16	577	147.5	138.0	76.2	16.2
17	575	147.5	137.0	75.7	16.1
18	576	150.5	139.5	75.6	16.4
19	573	147.0	136.5	76.2	16.0
20	574	148.0	138.0	76.3	16.2
21	576	149.0	139.0	76.1	16.3
22	574	147.0	136.5	76.0	16.0
23	575	149.0	139.0	76.3	16.3
24	575	148.5	138.5	76.2	16.3
25	575	149.5	139.5	76.3	16.4
Average	575	148.5	137.9	75.9	16.2

TABLE 7

ELECTRICAL PARAMETERS BEFORE AND AFTER AR COATING*

	BEFORE AR			AFTER AR			
Cell No.	Voc (mV)	Isc (mA)	Power (mW)	Voc (mV)	Isc (mA)	Power (mW)	Notes
01	599	164.0	74.6	590	179.8	79.8	MLAR
02	596	163.8	73.9	587	179.1	79.1	MLAR
03	598	165.0	73.5	587	179.4	79.1	MLAR
04	600	163.4	73.8	590	177.8	79.8	MLAR
05	601	163.6	74.0	590	177.8	78.7	MLAR
06	595	164.0	75.0	588	179.8	79.3	MLAR
07	602	164.1	75.4	590	178.6	80.0	MLAR
08	600	164.4	75.0	588	178.5	79.7	MLAR
09	600	164.7	75.0	590	179.3	80.3	MLAR
10	595	163.5	74.0	589	178.3	79.0	MLAR
Average	598.6	164.1	74.4	588.9	178.8	79.5	MLAR
11	599	164.4	74.2	588	174.9	77.2	SiO Coating
12	600	160.5	73.5	596	169.3	77.2	Spin-On AR

*@ 100 mW/cm^2, 28°C



Westinghouse) but after coating the Voc decreased by ~1.7% for MLAR and SiO, and by ≈0.7% for the spin-on AR. The result of this was that the Pmax increase was lower than expected because of reduction in Voc decrease. Table 7 gives some (values measured on a digital voltmeter) for these parameters; Figure 11 shows AMO I-V curves for coated and uncoated cells, including the red and blue components of the ASEC simulator. It can be seen that the Voc decrease is similar for all three illumination conditions, indicating that the change is not spectrally sensitive or intensity sensitive over a 2:1 range.

Dark forward diode characteristics showed decreased current at low voltages (50-450 mV) after AR coating. However, no changes were seen in the characteristics near cell operating conditions.

More tests are needed to explain this anomaly.

5.0 TOOLING AND EQUIPMENT

5.1 Back Contact Soldering Machine

The soldering machine as shown in Drawing No. D-202458, Sheets 1-3) is semi-automatic. It consists of a phenolic template with (120) 3" diameter cavities which accommodate the cells with mesh interconnects already soldered to the front contact. A Unitek resistance heating soldering machine mounted on two (2) 1 inch diameter steel rods was used. Indentations of 3.05" apart (3" diameter cell plus .050" spacing between cells) are provided on the rod. The soldering machine was manually moved from cell to cell, a step-repeat process. The fluxing and soldering

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TOP VIEW
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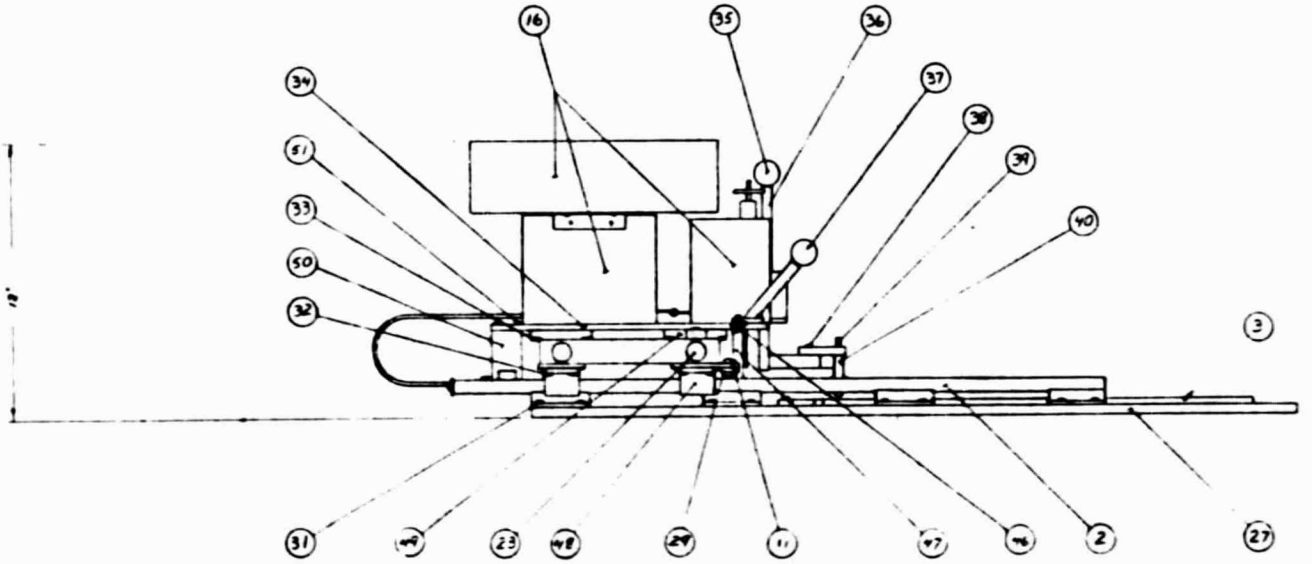


SIDE VIEW

REVISIONS					
ECO	DWG REV	LTR	DESCRIPTION	DATE	APPROVED
4260		A	INITIAL RELEASE	7-1-82	
5116		B	ADDED 2ND BASE	6-1-83	

ITEM	PART NO	DESCRIPTION	QTY
2		FLAT HEAD MACHINE SCREW 10-32 x 3/8"	98
1	8202407	EAGLE PULLEY MOUNT	97
9		"THUMB" ALLEN SCREW 8-32 x 1/2" LONG	96
3		"THUMB" ALLEN SCREW 8-32 x 1/2" LONG	95
1	8202466	EAGLE BUSHING MOUNT	94
9		SOCKET HEAD CAP SCREW 10-32 x 3/4"	93
4		FLAT HEAD MACHINE SCREW 8-32 x 1/2"	92

ITEM	PART NO	DESCRIPTION	QTY
10		HEX HEAD SOCKET HEAD CAP SCREW 8-32 x 3/8	95
2	8202443	SERVO-TECHNICAL SHAFT SPACERS	94
1		HEX HEAD SOCKET HEAD SHOULDER SCREW 8 x 1/2"	93
10		HEX HEAD SOCKET HEAD CAP SCREW 10-32 x 1/2"	92
2		VALVE NUT SCREW 8-32 x 3/8"	91
2	8202448	PLATE SUSPENSION SHAFT MOUNT	90
1		PIN - HOSE CONNECTOR ADAPTER, HOSE END	89
3		HEX HEAD SOCKET HEAD CAP SCREW 6-32 x 3/8"	88
1		PIVOT ARM SHAFT 1/2" DIAMETER BY 6" LONG	87
1	8202449	ACTUATOR ARM	86
1		ACTUATOR ARM SHAFT 1/2" DIAMETER BY 3" LONG	85
1	C202453	SUSPENSION SHAFT MOUNTING PLATE	84
12		HEX HEAD SOCKET HEAD CAP SCREW 10-32 x 3/8"	83
16		HEX HEAD SOCKET HEAD CAP SCREW 8-32 x 1/2"	82
16		HEX HEAD WASHER HEAD SCREW 8-32 x 3/8"	81
2		BEARING 3/8" ID x 5/8" DIAMETER	80
2	8202440	MOTOR MOUNT EXTENSION	79
8		[illegible]	78
1	C202454	BASE PLATE	77
1	B202455	FRONT CABLE SHAFT	76
2		DOWEL PIN 1/4" DIA 3/4" LONG	75
2	8202450	MOTOR MOUNT BLOCK	74
1	B202437	MODIFIED SERVO-TECHNICAL SHAFT	73
2	C202452	SIDE BAR	72
6		HEX HEAD SOCKET HEAD CAP SCREW 10-32 x 3/4"	71
1	B2424438	SERVO-TECHNICAL SHAFT	70
1	B202439	TERMINATE ADJUSTMENT BAR	69
1	B202447	ACTUATOR ARM MODIFIED ANGLE	68
6		HEX HEAD SOCKET HEAD CAP SCREW 10-32 x 1/2"	67
1		UNIVERSAL TRUNNION UNIT	66
2		HEX HEAD SOCKET HEAD CAP SCREW 10-32 x 1/2"	65
1	8202445	EAGLE SUPPORT	64
2		HEX HEAD SOCKET HEAD CAP SCREW 8-32 x 1/2"	63
1	8202442	SERVO-TECHNICAL STAR FOLLOW MOUNTING BLOCK	62
2		NYLON SPACE MACHINED TO Ø.400	61
4		HEX HEAD SOCKET HEAD CAP SCREW 10-32 x 5/8"	60
4		NYLON ROD Ø.250" x 1.00"	59
2	8202451	BASE MOUNT BLOCK	58
8		HEX HEAD SOCKET HEAD CAP SCREW 8-32 x 1/2"	57
4		SHOULDER SCREW 8-32 x 3/4"	56
1	B202460	SPACE ARM	55
1	B202444	FLAT HORIZONTAL SUPPORT ARM	54
1	MB4320	180 DEGREE SHIELDED PRECISION	53
1	B202457	LEFT CABLE SHAFT	52
8	8202439	SHAFT SUPPORT	51

DRAWN	
CHECKED	
ENGINEER	
MFG APPROVAL	
QA	
COMMENTS:	

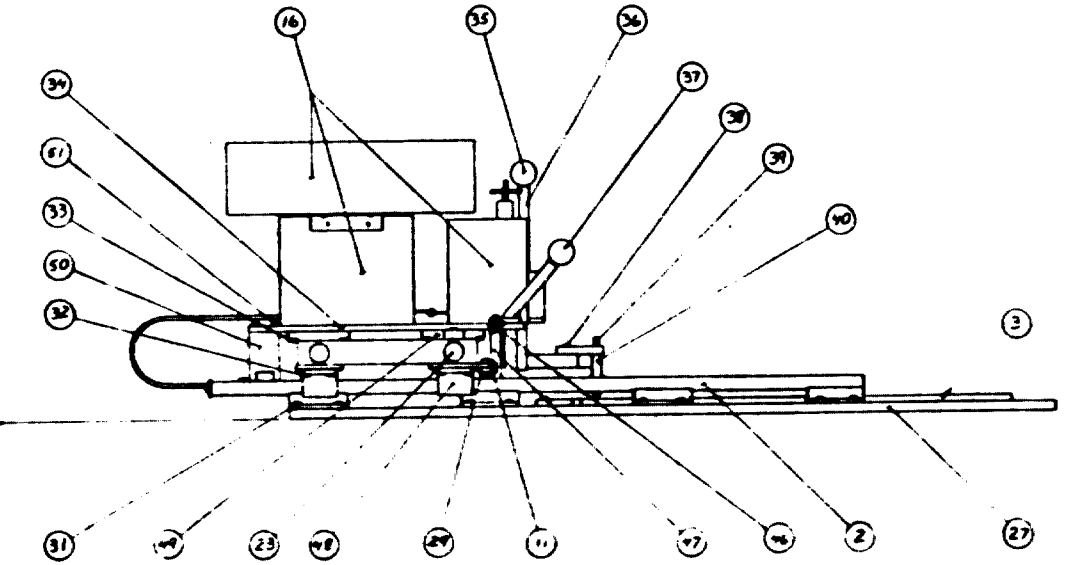
OCLI

Y-Y MOTION SOLDERING DEVICE

SIZE D | DWG NO C202458 | REV B

SCALE N/A | WEIGHT | SHEET 2 OF 3

NOTES: 1. ITEMS NOT IDENTIFIED ON THIS VIEW ARE ON OTHER VIEWS OF DRAWING.



SIDE VIEW

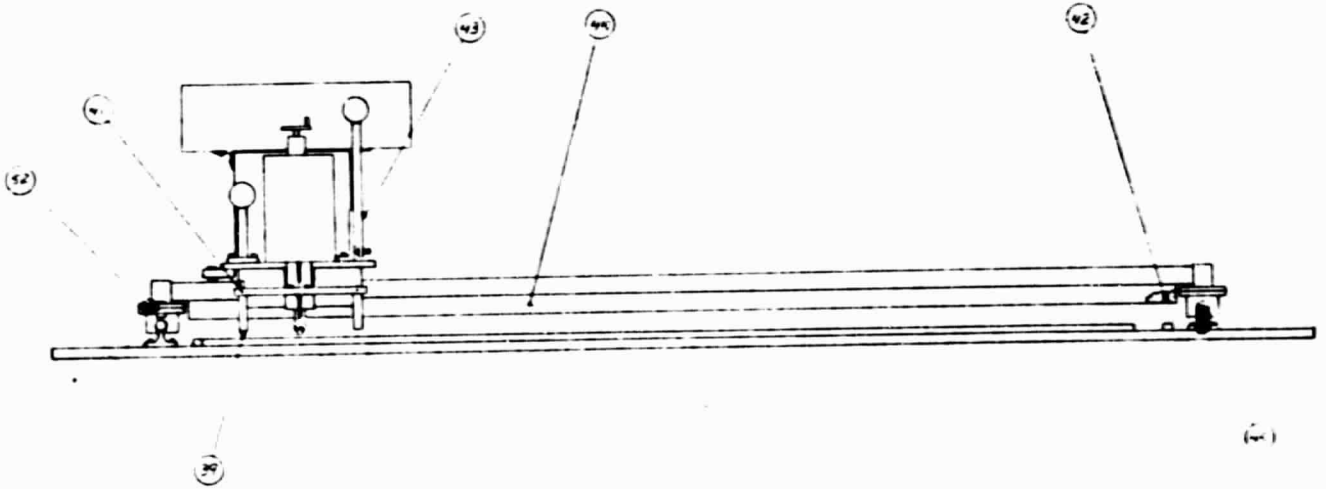
ITEM	PART NO.	DESCRIPTION	QTY
8			95
1			94
6			93
5			92
1			91
9			90
9			89

ITEM	PART NO.	DESCRIPTION	QTY
95			
94			2
93			1
92			10
91			2
90			2
89			1
88			3
87			1
86			1
85			1
84			1
83			12
82			16
81			16
80			2
79			2
78			1
77			1
76			2
75			2
74			1
73			2
72			6
71			1
70			1
69			1
68			6
67			1
66			2
65			1
64			2
63			4
62			4
61			2
60			8
59			7
58			1
57			1
56			1
55			1
54			1
53			1
52			1
51			1

OCU

V-Y MOTION SOLDERING DEVICE

C202458



FRONT VIEW

OCU
X-Y MOTION
SOLDERING DEVICE

was done automatically, with the exception that fluxing during the soldering of the parallel strings will be done manually.

The machine is designed to solder 15 cells in series and 8 cells in parallel. The sequence of soldering is as follows:

a) For Series Connections

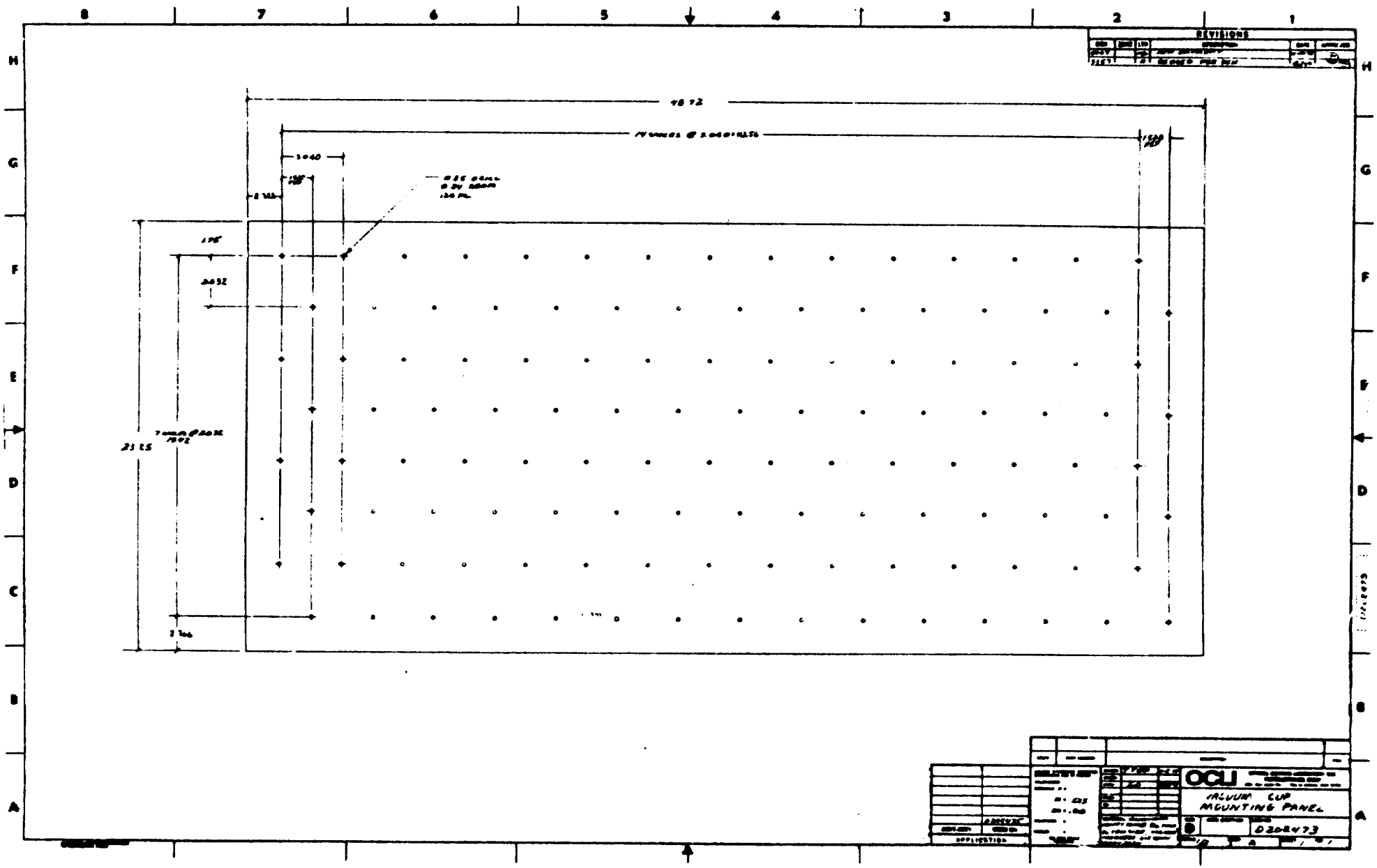
Place template against stop on left with "Y" motion in the first hole. Move soldering machine to the right in "X" direction in 3.05" increments until 15 cells are solder-connected in series. Move template to the right against stop which offsets the template by 1.525" and locates the staggered pattern of the next row. Move "Y" motion to the second hole and proceed with "X" motion to the left. Repeat above procedures until all 120 cells are soldered.

(b) For Parallel Connections

Remove dowel pin from stop on the right hand side and install the pin into the lower hole as appeared in the drawing. Move "X" and "Y" motions to their respective first hole. This will locate the first solder joint for the parallel circuit. A piece of copper mesh cut to the proper length is to be placed on the cells. Proceed to move "Y" motion into the second hole until 8 cells are connected in parallel. Move "X" motion to fifth, tenth, and fifteenth stop and repeat "Y" motion soldering.

5.2 Vacuum Pick-Up

To facilitate removal of the 120 cell assembly from the soldering template, a simple vacuum pick-up has been designed as shown in Drawing


REVISIONS
48.72
23.25
OCLI
VACUUM CUP
MOUNTING PANEL
D202473

Nos. D-202475 and D-202473. Two pieces of aluminum honeycomb, spaced 1/16" apart were edge-sealed. One hundred and twenty (120) soft vacuum cups were inserted into one side of the honeycomb. Each cup was positioned over the bare contact of the cell. A vacuum valve was installed on the opposite side. The in-house central vacuum system (30 inches Hg) was used to operate the pick-up.

This piece of equipment proved to be quite valuable during this contract. It was used not only for pick-up from the template, but also as a method of holding the textured cell soldered array when drying after the flux removal washing operation..

5.3 AR Coating Tooling

The evaporator used for applying multi-layer anti-reflective coating has five (5) pie shaped plates, each holding eleven (11) 3" cells. The center contact of the cell must be shielded during AR coating evaporation to provide solderability. Small, high power magnets were found to work satisfactorily on a limited basis. There magnets were Hicorex permanent magnets (a cobalt rare earth material) that are quite strong at room temperature. It was soon found, however, that they lost considerable power at the elevated temperature required for the multi-laryer evaporation process. We improved the system in two ways. First another magnet was placed on the back of the cell to increase the magnetic field. Then spring loaded clips were added to hold the wafer in place even if the magnet didn't hold. This system also failed because even though the wafer stayed in place the magnet mask still fell off and allowed AR coating to deposit on the center contact. The final and most successful

method found was to use the spring clips to hold wafers in place then apply a dot of high temperature tape over the center contact. The tape worked very well and the extra labor involved was found to be much more economical than the magnetic approach.

5.4 Test Fixture

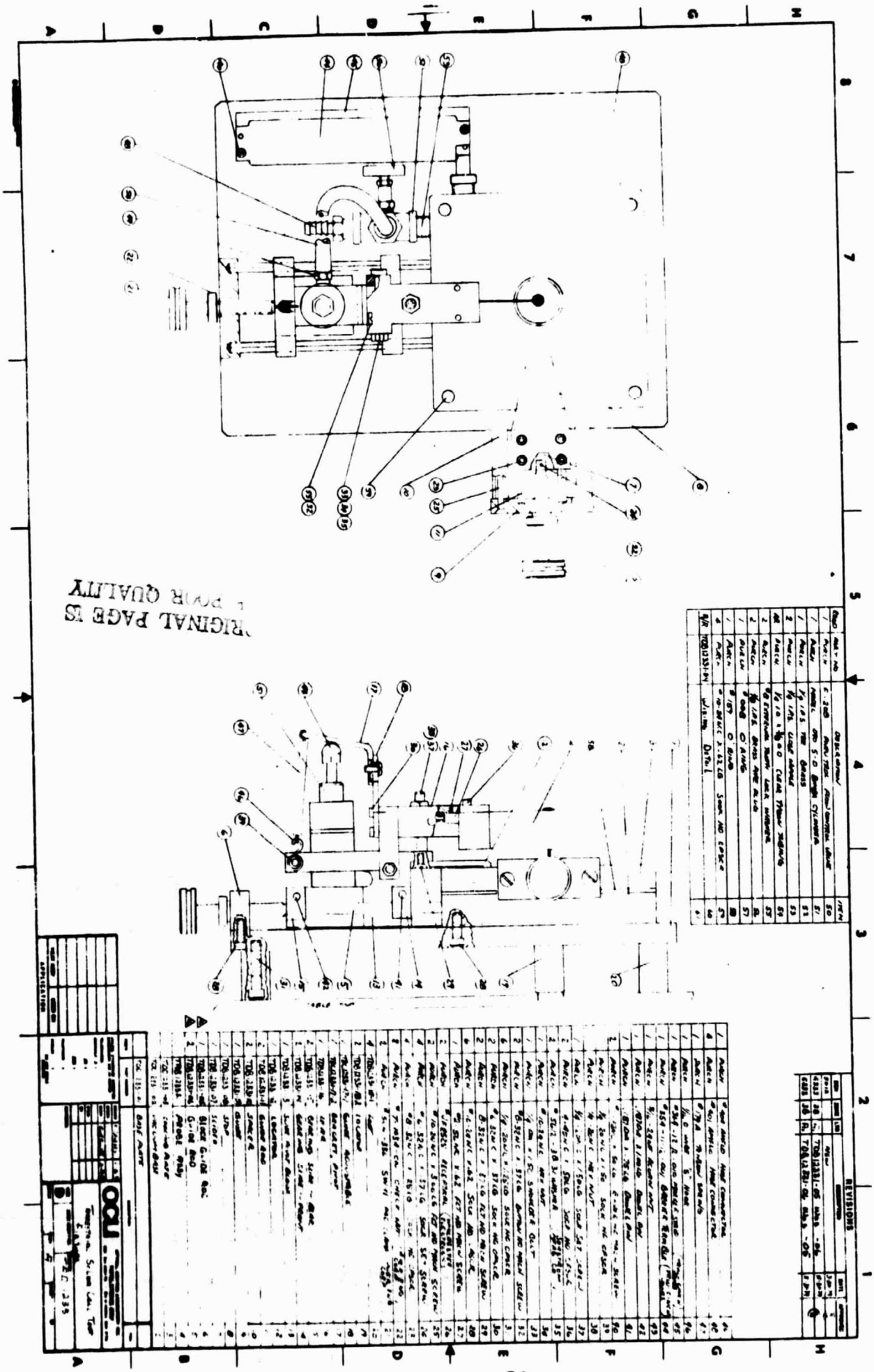
The test fixture, as shown in Drawing No. TAD-12331, utilizes the existing design modified for the center contact cells. Narrow current voltage probes, electrically isolated, made contact to the cell. The test fixture also has provisions for cooling fluid to control temperature, vacuum hold down, thermocouple, and a solenoid to operate the probes. The fixture is capable of testing cells up to 5" in diameter. All electrical contact areas are gold plated to insure maximum current carrying and minimum resistance. The probe location can be adjusted in both X and Y directions with the micro slide adjusting screws. The fixture is compact in size and can easily be adapted to any light source.

6.0 CONCLUSIONS AND RECOMMENDATIONS

6.1 Conclusions

This program demonstrated that large area P+NN+ cells of high efficiency could be fabricated, and combined successfully into modules, with the same effectiveness as N+PP+ cells.

The desired cell performance goals were met by several experimental lots of smaller cells (area $\sim 4cm^2$). Problems were found in achieving the same high efficiencies for 3" diameter cells, but the reasons



were mainly in the formation of the shallow P+ layer. Even so, 1000 cells, with average efficiency 13.5% were made and used in the delivered arrays.

The main conclusion is that if low cost N-silicon of reasonable quality should become available, it is possible to fabricate high output modules using this silicon.

6.2 Recommendations

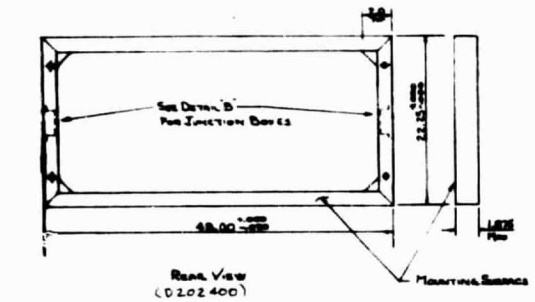
As mentioned, the module design and fabrication were most satisfactory. The main area requiring slight improvement is to continue the development (completed in this contract) of high efficiency, large area P+NN+ cells. The main areas requiring additional development are:

- Improved boron diffusion conditions.
- Slightly improved N+ layer formation.
- Replace BSF structure, with P+NN+ cells with N-silicon 2 ohm-cm, and the N+ layer not a BSF.

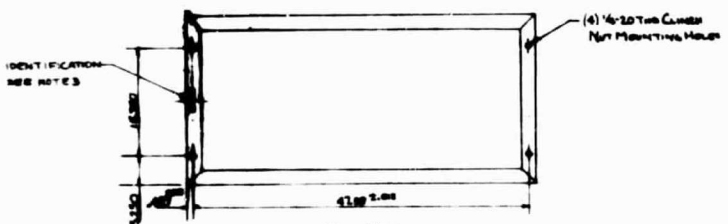
A limited program could check these predictions, and provide a firm basis for possible future need for high efficiency P+NN+ cells. The suggested areas of research can also take advantage of concurrent work on P+NN+ concentrator cells.

7.0 REFERENCES

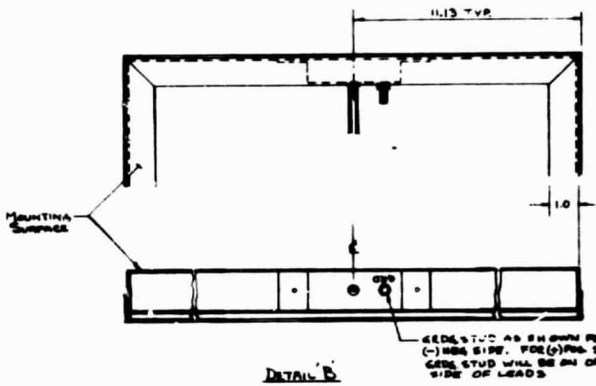
1. Various work under JPL Lithium Program (unpublished).
2. "P/N High Efficiency Silicon Solar Cells", M.S. Bae and R.V. D'Aiello, Appl. Phys. Lettr, 31, No. 4, 1977, P.265.
3. "High Efficiency P+NN+ Back-Surface-Field Silicon Solar Cells", J.G. Fossum and E.L. Burgess, Appl. Phys.Lettr, 33, No.3,1978,P.238.



Rear View
(D202400)



Rear View
Mounting Hole Locations
(D202400)



Detail 'B'

Notes:
1. Resistance Welded Aluminum Frame Assembly
2. Anodized Finish
3. Module Identification Label Located On Glass (Front Side)
4. Nominal Estimated Weight = 24#
5. Estimated Performance Data:
   Average Output [illegible] With Insolation Of 100 MW/CM² At
   28°C ± 2°C; [illegible]
6. Out Put Termination (2) #16 AWG Teflon Insulated Wires 48" Lg Ads
   Supplied For Each Polarity. The (2) White Ads (+) & (2) Black Ads (-)
   These Pigtails Are Furnished Fully Interconnected & Cut To Length.
   A #6-32 x 1/2 Lg Stainless Steel Grounding Stud With Hex Lock Nut Is Also Furnished

ORIGINAL PAGE IS
OF POOR QUALITY

-53-

REVISIONS				
		A	[illegible]	
		B	REVISED PER DCN [illegible]	

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D202390